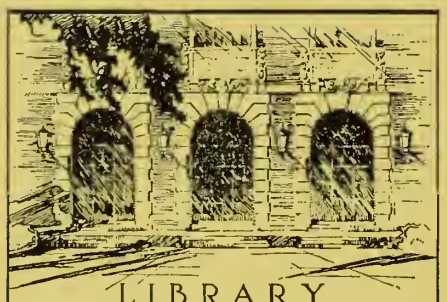

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SWITCHING-MODE AUDIO AMPLIFIER

by

James E. Selleck

June 1, 1967

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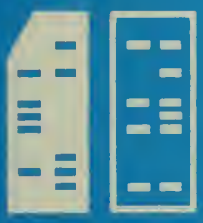

DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

Report No. 229

SWITCHING-MODE AUDIO AMPLIFIER†

by

James E. Selleck

June 1, 1967

Department of Computer Science
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Urbana, Illinois 61801

† Submitted in partial fulfillment of the Master of Science degree in Electrical Engineering, June 1967.

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1. STATEMENT OF PURPOSE AND INTRODUCTION

The purpose of the paper is to show the system equations, design method, and a working model of an audio amplifier operating in the switching mode.

The principle of complementary switching for an audio power amplifier was developed by Mr. A. G. Bose (See References 2, 3, and 4) of MIT Research Laboratory of Electronics. Mr. Bose used a non-linear forward path network and a linear feedback network, while this paper uses a local sawtooth generator for better linearity and for higher percentage of modulation.

After a low power audio signal is converted to a single-edge modulated square wave, switching circuit technology is used to power amplify the resulting square wave. Finally, the amplified audio signal is recovered by using a detector.

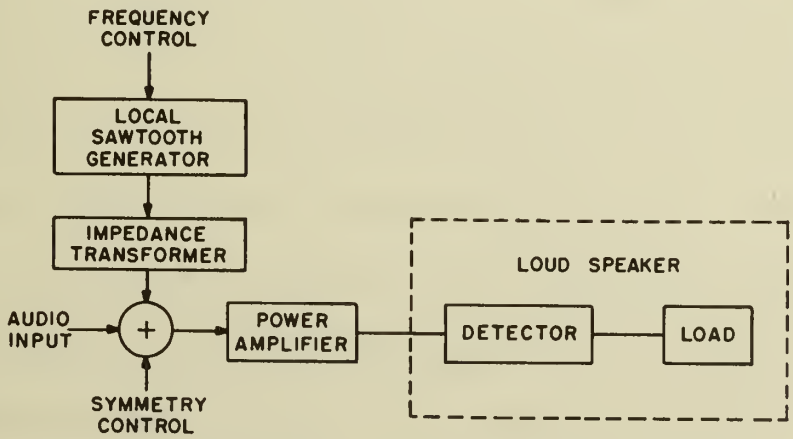


FIGURE 1

SWITCHING-MODE AUDIO AMPLIFIER SYSTEM DIAGRAM

A local sawtooth generator, with a frequency control, generates a linear ramp with a repetition rate about ten times the highest audio frequency to be amplified. The impedance transformer prevents loading on the sawtooth generator thereby improving the linearity of the sawtooth ramp and drives the low input impedance summing circuit.

The summing circuit driving the complementary switching power amplifier develops a square wave output. The symmetry control adjusts the square wave output to the symmetrical state when no audio signal is applied to the summing network. When an audio signal is added to the sawtooth wave and the symmetry control level, a single-edge modulated square wave is developed at the output of the power amplifier. The time period of the square wave is fixed by the fly-back of the sawtooth wave, the amplitude information of the audio signal is in the asymmetry of the square wave, and the frequency information of the audio signal is in the rate of change in the asymmetry of the square wave. A low-pass filter detects the amplified audio signal from the edge modulated square wave. For this investigation a low-pass filter and a resistive load is used in the model, but in actual system application a loudspeaker can be used for the low-pass filter as well as the output device.

The local sawtooth generator method of modulation is advantageous, because the modulation is on a linear ramp instead of a nonlinear signal such as sinusoidal or exponential. The linear ramp allows higher per cent of modulation and low carrier signal frequency for the

same audio signal range. A current feedback pair is used in the summing circuit, because the very low input impedance minimizes the interaction between the two input signals. The power amplifier's transistors are in either the cut-off or saturation states for minimization of the device power dissipation. Therefore, larger signal powers can be handled with low power high frequency devices.

2. THEORY AND DESIGN

Local Sawtooth Generator

The local sawtooth generator is an asymmetrical multivibrator with a current source (transistor T_3 in Figure 2) replacing one base resistor. With a constant-current charging a capacitor, a linear voltage ramp is generated. The other side of the multivibrator generates the fly-back of the sawtooth generator.

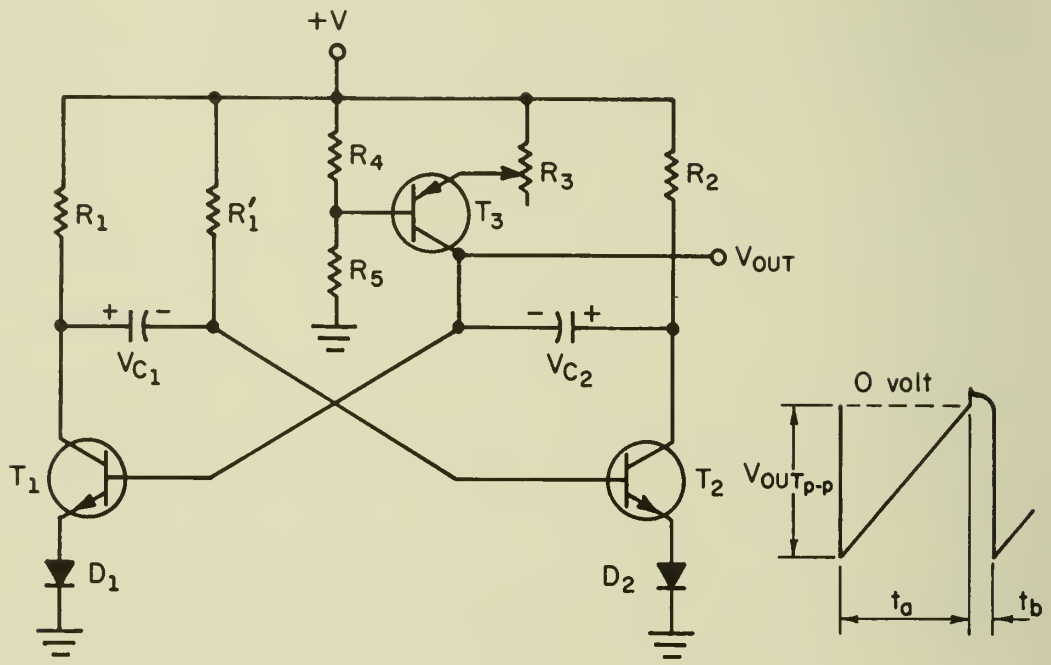


FIGURE 2 LOCAL SAWTOOTH GENERATOR

The period of one complete cycle of the sawtooth is

$t_o = t_a + t_b \approx \frac{1}{10 \times f_{A_{MAX}}}$, where $f_{A_{MAX}}$ = maximum audio to be amplified.

During time period t_a (ramp), transistor T_1 is off and transistor T_2 is saturated. Capacitor C_1's time constant is:

$$t_1 = R_1 C_1$$

and capacitor C_2 is being charged by a constant-current I. During time period t_b (fly-back), transistor T_1 is saturated, and transistor T_2 is off. The time constant of capacitor C_1 is:

$$t_1' = R_1' C_1$$

and the time constant of capacitor C_2 is:

$$t_2' = R_2 C_2$$

The frequency of the sawtooth generator and the allowed asymmetry of the generator output determines the times t_a and t_b.

$$t_a + t_b = t_o = \frac{1}{fg}$$

and the asymmetry is defined as:

$$A_o = \frac{t_o/2 - t_b}{t_o/2} \times 100 \quad \therefore \quad t_b = \frac{t_o}{2}\left[1 - \frac{A_o}{100}\right]$$

$$R_1 = R_2 = \frac{+V}{I_{C_{MAX}}}$$

where $I_{C_{MAX}}$ is the maximum saturation collector current for transistors T_1 and T_2. Matching the boundary conditions at the completion of

time t_b:

$$V_{C_2} = +V\ (1 \quad e^{-t/t_2'})$$

when $t = t_b, V_{OUT} = -V_{C_2}$

$$t_2' = t_b \ln \left[1 - \frac{V_{OUT_{p-p}}}{+V} \right] \text{ and } C_2 = \frac{t_2'}{R_2}$$

Matching the boundary conditions at the completion of time t_a:

When $t = t_a +$, $V_{C_1} = 0$ at when $t = t_a -$, $V_{C_1} = +V\ (1-e^{-t_a/t_1})$

$$V_{C_1} = 0 = -V_{C_1} + (V_{C_1} + V)\ (1-e^{-t_b/t_1'})$$

$$0 = -V\ (1-e^{-t_a/t_1}) + V\ (2-e^{-t_a/t_1})\ (1-e^{-t_b/t_1'})$$

$$0 = e^{-t_b/t_1'} - 2 + e^{-t_a/t_1}$$

where $t_1 = R_1C_1$ and $t_1' = R_1'C_1$

For normal operation of transistor T_1, the base resistance R_1' is more than an order of magnitude larger than the collector resistance R_1. The asymmetry of the multivibrator is desired for the sawtooth generator for minimization of the fly-back time (larger percent of modulation). Therefore, t_b is less than t_a.

$$\therefore \left| \frac{t_b}{t_1'} \right| \angle\angle \left| \frac{t_a}{t_1} \right|$$

The controlling factor in the resulting boundary equation is the positive exponent.

$$e^{+t_b/t_1'} = 2$$

$$t_o = t_a + t_b,\ A_o = \frac{t_o/2 - t_b}{t_o/2} \times 100$$

$$t_b = \frac{t_o}{2}\left[1 - \frac{A_o}{100}\right]$$

$$t_b = \frac{t_1'}{\ln 2}$$

$$C_2 = \frac{t_b}{R_2} \ln\left[1 - \frac{V_{OUT_{p-p}}}{V}\right] =$$

$$\frac{t_o}{2R_2}\left[1 - \frac{A_o}{100}\right] \ln\left[1 - \frac{V_{OUT_{p-p}}}{V}\right]$$

$$C_1 = \frac{t_b}{R_1' \ln 2} = \frac{1}{R_1' \ln 2} \times \frac{t_o}{2}\left[1 - \frac{A_o}{100}\right]$$

$$f_{A_{MAX}} = 20\ KC, \quad \therefore\ t_o = \frac{1}{200 \times 10^3} =$$

$$5. \times 10^{-6} = 5\ \mu sec.$$

With a 12 volt supply and 6 volt peak-to-peak output.

$$I_{C_{MAX}} = 300\ ma, \quad \therefore\ R_1 = R_2 = + \frac{12V}{300\ ma} = 400\Omega$$

Let $R_1 = R_2 = 390\Omega$

For these operating conditions, the maximum percentage of asymmetry is 80 per cent which results in approximately 80 per cent maximum modulation later in the system. The output voltage decreases with increase in percentage of asymmetry.

$$R_1' = R_1 \times h_{FE_{MIN}} = (390\,\Omega) \times 20 = 7.8K$$

Let $R_1' = 7.5K$

$$C_2 = \frac{t_o}{2R_2}\left[1 - \frac{A_o}{100}\right] \ln\left[1 - \frac{V_{OUT_{p-p}}}{V}\right] = 1.85 \times 10^{-9}$$

Let $C_2 = 1.8$ nf.

$$C_1 = \frac{1}{R_1' \ln 2} \times \frac{t_o}{2}\left[1 - \frac{A_o}{100}\right] = 96.2 \times 10^{-12}$$

Let $C_1 = 100$ pf.

$$I \text{ (charging current)} = \frac{C_2 \times V_{C2_{p-p}}}{t_a} = 2.4 \text{ ma.}$$

Let $V_{B_{T3}} \approx$ 6 volt to insure T_3 is operating in the linear region.

$$R_3 = \frac{h_{FE}}{1 + h_{FE}}\left[\frac{V - V_{BT3} - V_{BET3}}{1}\right] = 2.32 \times 10^{+3}$$

Use a 5K ohm variable resistance for the frequency control.

Impedance Transformer

The requirements for the impedance transformer circuit are: minimum loading on the sawtooth generator, ability to drive a low

input impedance summing circuit, and linear operation with large signal input. The circuit configuration to meet these requirements is a voltage feedback pair with unity feedback. The feedback pair has better linearity during large signal operation than a Darlington network.

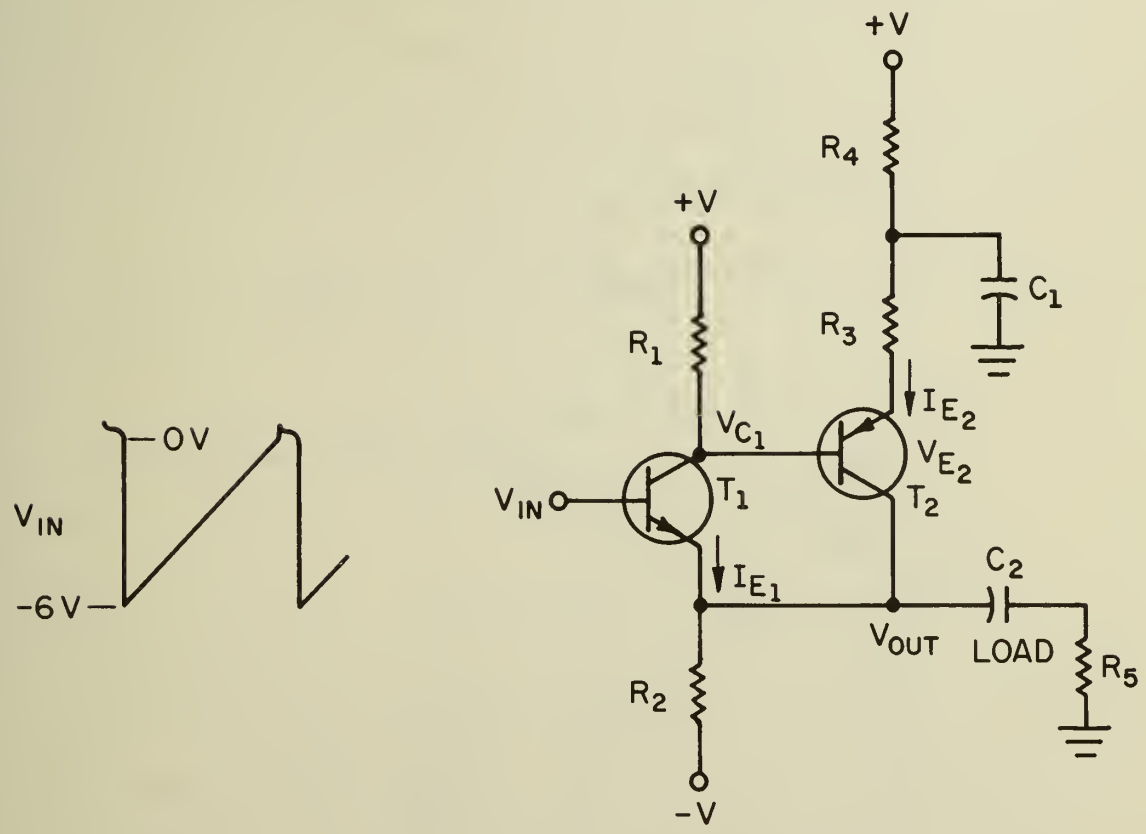


FIGURE 3 IMPEDANCE TRANSFORMER

The dc circuit equations are:

$$V_{C_1} = V - \left[\frac{h_{FE}}{1 + h_{FE}}\right] I_{E_1} R_1$$

$$V_{E_2} = V_{C_1} - V_{B_2} = V - (R_3 + R_4) I_{E_2}$$

$$V_{OUT} = V_{IN} - V_{BE_1} = R_2 \left[I_{E_1} + \frac{h_{FE}}{1 + h_{FE}} I_{E_2}\right] - V$$

The dc design criteria are that V_{C_1} be approximately equal to plus six volts when V_{IN} is at its most positive level for linear transistor operation, and that the emitter current of the first transistor equals the collector current of the second transistor to balance the output voltage sensitivity between the two transistors.

$R_1 = 1200$ ohm

$R_3 + R_4 = 1100$ ohm

$R_2 = 1100$ ohm

The value of R_3 was derived by using the Steady-State AC Network Analysis Program (SSNA) with the performance criteria of: stable input impedance, maximum input impedance, and minimum output impedance. The program was also used to select the value of C_1 based on the criterion of minimum capacitance with less than one per cent effect on the sawtooth fundamental.

Summing Network

The function of the summing network is to add electronically the sawtooth and the audio signals. The audio signal would normally come from a preamplifier that has an output dc level of +9 volts and low ac output impedance. The summing network was designed on the computer with the following circuit topology and component and operation point limitation.

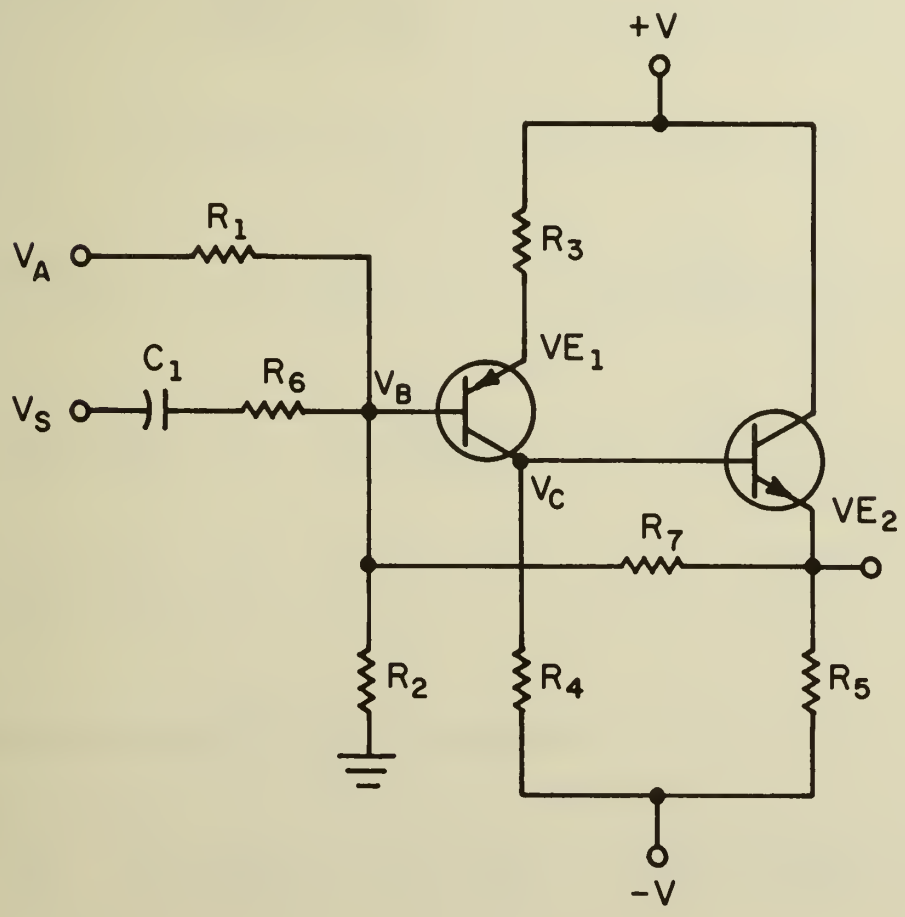


FIGURE 4 SUMMING NETWORK

$1.0K \leq R_1 \leq 10.K$

$0.5K \leq R_2 \leq 10.K$

$25\,\Omega \leq R_3 \leq 5.K$

$100\,\Omega \leq R_4 \leq 5.K$

$100\,\Omega \leq R_5 \leq 10.K$

$100\,\Omega \leq R_7 \leq 10.K$

All resistors are 5 per cent tolerance of selected values.

$30 \leq HFE_1 \leq 150$ PNP transistor

$30 \leq HFE_2 \leq 150$ NPN transistor

$(VE_1 - VC) \geq 5$ volt

$(VC - VE_2) \geq .7$ volt

$I_{R_3} \leq 10$ ma

2 ma $\leq I_{R_5} \leq 10$ ma

	STATE 1	STATE 2
V_A (audio input dc level)	+9.9 volt	+8.1 volt
V (+12) supply voltage	+11.4 volt	+12.6 volt
V (-12) supply voltage	-12.6 volt	-11.4 volt

The following equations were generated by the Automatic Circuit Optimum Program (ACOP) written by Mr. A. G. Kennard, IBM, Systems Development Division, Poughkeepsie, New York.

$$A1 = \frac{HFE_1}{1 + HFE_1}$$

$$A2 = \frac{HFE_2}{1 + HFE_2}$$

$$C1 = \frac{1}{R_5} + \frac{1}{R_7} + \frac{1}{HIE_2}$$

$$C2 = \left[\frac{V\ (-12)}{R_5} - \frac{VBE_2}{HIE_2}\right] \times \frac{1}{C1}$$

$$C3 = \frac{1}{R_3} + \frac{1}{HIE_1}$$

$$C4 = \left[\frac{V\ (+12)}{R_3} + \frac{VBE_1}{HIE_1}\right] \times \frac{1}{C3}$$

$$C5 = \frac{1}{R_4} + \frac{HIE_2 \times C1 - 1}{HIE_2^2 \times (1 + HFE_2) \times C1}$$

$$C6 = \left[\frac{V\ (-12)}{R_4} + \frac{(C4 - VBE_1) \times A1}{HIE_1} + \frac{C2 + VBE_2}{HIE_2 \times (1+HFE_2)}\right] \times \frac{1}{C5}$$

$$D = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_7} - \frac{1}{R_7^2 \times C1} + \frac{HIE_1 \times C3 - 1}{HIE_1^2 \times C3 \times (1+HFE_1)}$$

$$+ \frac{A1}{HIE_1 \times HIE_2 \times C1 \times C5 \times R_7} - \frac{1}{R_7^2 \times C1^2 \times HIE_2^2 \times C5 \times (1+HFE_2)}$$

$$- \frac{A1}{R_7 \times C1 \times HIE_2 \times C5 \times C3 \times HIE_1^2}$$

$$VB = \left[\frac{VA}{R_1} + \left(\frac{C6}{C1 \times HIE_2} + C2\right) \times \frac{1}{R_7} + \frac{C4 - VBE_1}{HIE_1 \times (1+HFE_1)}\right] \times \frac{1}{D}$$

$$VC = \left[-\frac{VB \times A1}{HIE_1} + \frac{VB \times A1}{HIE_1^2 \times C3} + \frac{VB}{R_7 \times C1 \times HIE_2 \times (1+HFE_2)}\right] \times \frac{1}{C5} + C6$$

$$VE_1 = \frac{VB}{HIE_1 \times C3} + C4$$

$$VE_2 = \left[\frac{VB}{R_7} + \frac{VC}{HIE_2}\right] \times \frac{1}{C1} + C2$$

Then the program randomly selects circuit components between the specified limits. The circuit components that gave the minimum value for delta are used as starting values where delta is defined as:

$$DELTA = \left|VE_2 \text{ (state 2)} - VE_2 \text{ (state 1)}\right| \times 10^4 + \left|VE_2 \text{ (state 2)}\right| \times 10^5 + \left|VE_2 \text{ (state 1)}\right| \times 10^5$$

The program then does a direct search to minimize the variable delta. The purpose of the delta function is to design a circuit whose output voltage is near zero and then minimize the difference between these two states of the output voltage. See Appendix B for examples of the computer printout.

The computer program SSNA was used to design C1 for less than .1 per cent change in the phase angle of the voltage transfer function for the sawtooth input. The resulting component values were:

R_1 — 2.0K

R_2 — 6.2K

R_3 — 1.6K

R_4 — 2.7K

R_5 — 4.3K

R_6 — 2.0K

R_7 — 7.5K

C1 — 100 nf

The resistor R_4 is changed to a 5000 ohm variable resistor to control the output dc level (symmetry control). The use of this variable resistor is covered later in the power amplifier section.

Power Amplifier

The power amplifier has two functions: zero crossing detection and power amplification. The output dc level of the summing network, with no audio signal input, is adjusted by the symmetry control to the position with half of the time base of the sawtooth signal below zero and half above zero. Then as the audio signal is applied, the zero crossing of the sawtooth is modulated along the time base. The first stage of the power amplifier is a complementary switching circuit which detects the zero crossing. The first two diodes minimize the zero crossing detection zone, plus removing the requirement for the summing circuit to supply the power amplifier base current. The second stage of the power amplifier delivers the high power square wave to the load network. The second pair of diodes limits the base current and limits the reverse voltage on the base-emitter junction of the output transistors.

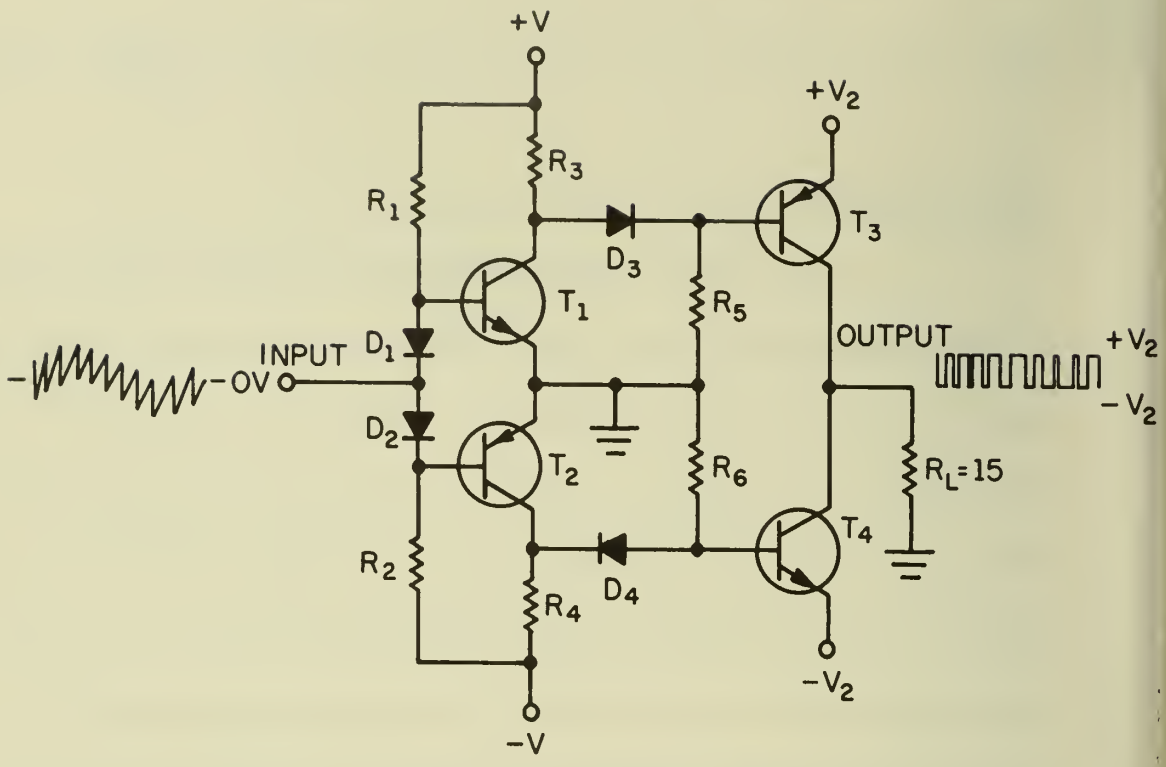


FIGURE 5 POWER AMPLIFIER

The dc design equations for the power amplifier are:

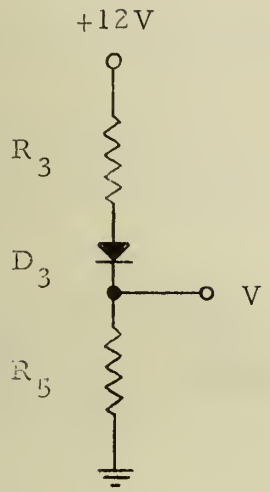
For transistors T_3 and T_4

$$I_{CON} = \frac{5V - V_{CE\ SAT}}{R_L} = \frac{5.0 - 1.0}{15} = \frac{4.0}{15} = 267\ ma$$

$$R_5 = R_6 \quad \frac{5V - V_{BE\ SAT}}{I_{CON}/hFE_{MIN}} = \frac{5 - .8V}{267\ ma/25} = 393\,\Omega$$

Let $R_5 = R_6 = 390\,\Omega$

When transistors T_1 and T_3 are OFF



$$V = \frac{R_5}{R_3 + R_5} (12V - V_{D_3}) \geq +5 \text{ volt}$$

Let $R_3 = R_5 = 390\,\Omega$, $V_{D_3} = .8$ volt

$V = 1/2\ (11.2) = 5.6$ volts $\geq +5$ volt

For transistors T_1 and T_2

$$I_{C_{ON}} = \frac{+12V - V_{CE\ SAT}}{R_3} = \frac{12 - .3}{390} = 30.3 \text{ ma}$$

$$R_1 = R_2 = \frac{12V - V_{BE\ SAT}}{I_{C_{ON}}/h_{FE_{MIN}}} = \frac{12 - .3}{30.3/25} = 9,669\,\Omega$$

Let $R_1 = R_2 = 10K$

Transistor Power:

T_1 and T_2 $\quad P = 1/2\ (I_B V_{BE} + I_C V_{CE}) = 3.21$ mwatt

T_3 and T_4 $\quad P = 1/2\ (I_B V_{BE} + I_C V_{CE}) = 137.8$ mwatt

Detector

A low pass filter attenuates the square wave and passes the amplified audio signal.

$$Z_o = 15\Omega = R_o$$

$$L_o = \frac{Z_o}{\pi f_C}, \quad C_o = \frac{1}{\pi Z_o f_C}$$

$$m = \sqrt{1 - \left[\frac{f_C}{f_\infty}\right]^2} \qquad \text{(See References 6, 10, 11)}$$

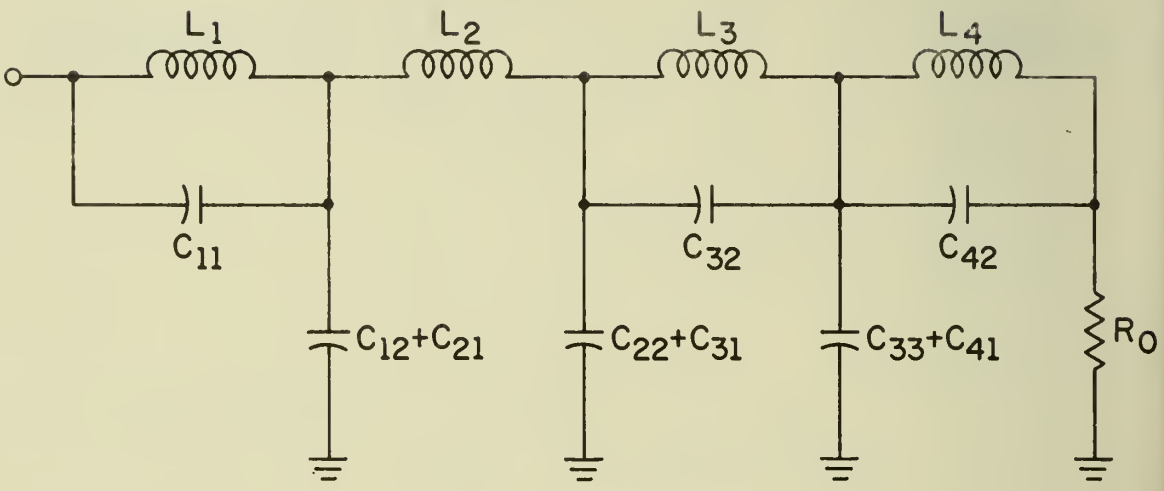


FIGURE 6 LOW PASS FILTER

Section	fC	f_∞	m
1	152KC	190KC	0.600
2	180KC	------	-----
3	180KC	200KC	0.436
4	158KC	210KC	0.600

$$L_1 = m_1 L_{o_1}/2 = 9.4\,\mu h$$

$$C_{11} = \left[\frac{1 - m_1^2}{2m_1}\right] C_{o_1} = 74.5\ nf$$

$$C_{12} + C_{21} = \frac{m_1 C_{o1}}{2} + \frac{C_{o2}}{2} = 101.33\ nf$$

$$L_2 = L_{o2} = 26.5\ \mu h$$

$$C_{22} + C_{31} = \frac{C_{o2}}{2} + \frac{m_3 C_{o3}}{2} = 85.37\ nf$$

$$L_3 = m_3 L_{o3} = 10.6\ \mu h$$

$$C_{32} = \left[\frac{1 - m_3^2}{4 m_3}\right] C_{o3} = 55.2\ nf$$

$$C_{33} + C_{41} = \frac{m_3 C_{o3}}{2} + \frac{m_4 C_{o4}}{2} = 63.81\ nf$$

$$L_4 = \frac{m_4 L_{o4}}{2} = 8.5\ \mu h$$

$$C_{42} = \left[\frac{1 - m_4^2}{2 m_4}\right] C_{o4} = 67.4\ nf$$

Component values after tunning with SSNA and winding the four inductors are:

L_1	0.06Ω	14.4μh
C_{11}	75. nf	
$C_{12} + C_{21}$	100. nf	
L_2	0.10Ω	25.6 μh
$C_{22} + C_{31}$	82. nf	
L_3	0.05Ω	9.7 μh
C_{32}	56. nf	
$C_{33} + C_{41}$	62. nf	
L_4	0.04Ω	8.9 μh
C_{42}	68. nf	
R_o	15Ω	

The Overall Amplifier Response

The complete amplifier circuit that was described in the previous sections is shown in Figure 7. The power gain of the amplifier is defined as:

$$10 \log \left[\frac{V_{OUT}^2}{R_L} \times \frac{R_{IN}}{V_{IN}^2} \right]$$

The voltage gain of the amplifier consists of three parts: gain of the summing network, gain of the power amplifier, and the gain of the detector. The first and last gains are normal sinusoidal network gains, but the power amplifier's output is a modulated signal.

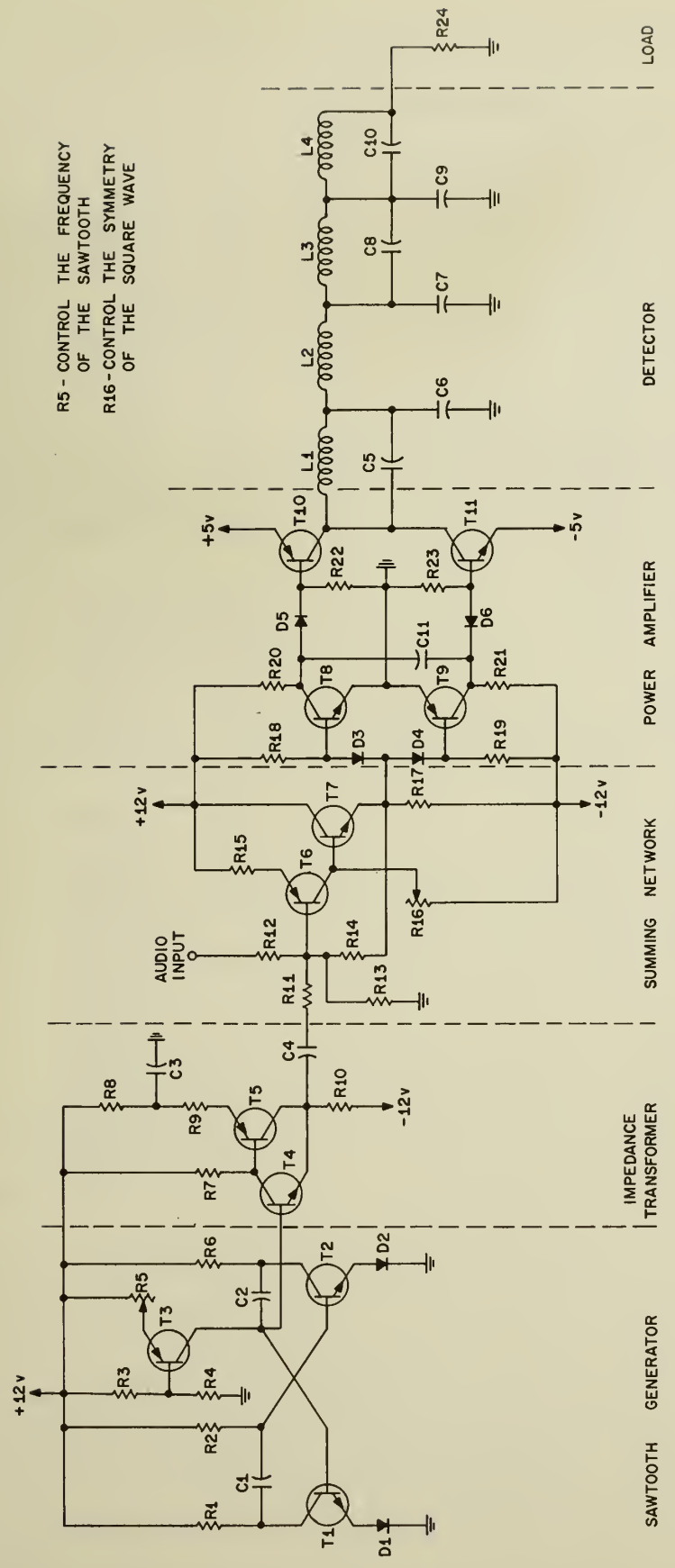


FIGURE 7 SWITCHING-MODE AUDIO AMPLIFIER

COMPONENT LIST

R1	390Ω, 1/2W, 5%
R2	7.5K, 1/4W, 5%
R3	4.7K, 1/4W, 5%
R4	4.7K, 1/4W, 5%
R5	0-5K , Variable
R6	390Ω, 1/2W, 5%
R7	1.2K, 1/4W, 5%
R8	910Ω, 1/4W, 5%
R9	200Ω, 1/4W, 5%
R10	1.1K, 1/4W, 5%
R11	2.0K, 1/4W, 5%
R12	2.0K, 1/4W, 5%
R13	6.2K, 1/4W, 5%
R14	7.5K, 1/4W, 5%
R15	1.6K, 1/4W, 5%
R16	0-5K , Variable
R17	4.3K, 1/4W, 5%
R18	10 K, 1/4W, 5%
R19	10 K, 1/4W, 5%
R20	390Ω, 1/2W, 5%
R21	390Ω, 1/2W, 5%
R22	390Ω, 1/2W, 5%
R23	390Ω, 1/2W, 5%
R24	15Ω , 2W , 5%

L1	.06Ω, 14.4 μh
L2	.10Ω, 25.6 μh
L3	.05Ω, 9.7 μh
L4	.04Ω, 8.9 μh

C1	100pf, 5%
C2	1.8nf, 5%
C3	50 nf, 20%
C4	100nf, 20%
C5	75 nf, 5%
C6	100nf, 10%
C7	82 nf, 5%
C8	56 nf, 5%
C9	62 nf, 5%
C10	68 nf, 10%
C11	240pf, 10%

D1	1N916
D2	1N916
D3	1N294
D4	1N294
D5	1N4244
D6	1N4244

T1	2N706
T2	2N706
T3	2N705
T4	2N705
T5	2N705
T6	2N705
T7	2N706
T8	2N955
T9	2N705
T10	2N2904
T11	2N3299

The modulation equation for trailing-edge modulation (See Reference 1) is:

$$V_o(t) = MV_2 \cos w_a t + 2V_2 \sum_{m=1}^{\infty} \frac{\sin m w_c t}{m}$$

$$-2V_2 \sum_{m=1}^{\infty} \frac{J_o(m\pi M)}{m\pi} \sin(m w_c t - m\pi)$$

$$-2V_2 \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm \infty} J_n \frac{(m\pi M)}{m\pi} \sin\left(m w_c t + n w_a t - m\pi - \frac{n\pi w_a}{2}\right)$$

where: $M = \dfrac{V_{p\text{-}p \text{ audio}}}{V_{p\text{-}p \text{ sawtooth}}}$

$f(w_a)$ = normalized audio signal = $M \cos w_a t$

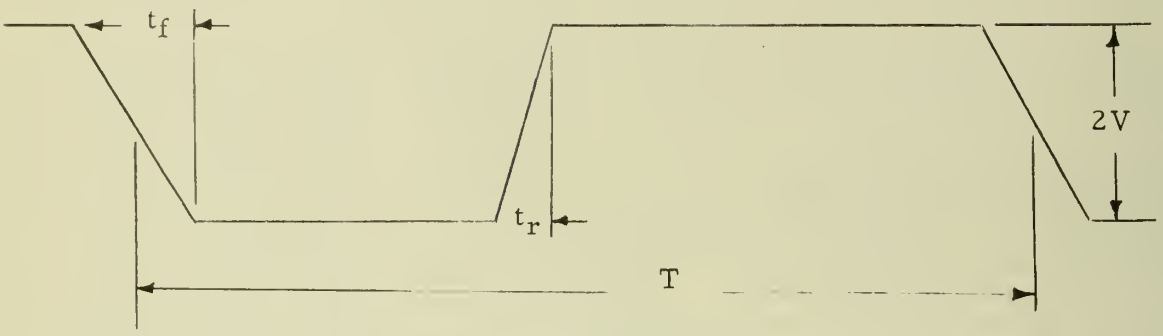
$V_{\text{output}_{p\text{-}p}} = 2V_2$

w_a = angular frequency of the audio signal

w_c = angular frequency of the sawtooth signal

The summing network gain is the same for the audio signal as for the sawtooth; therefore, the amplitude ratio is measured at the input to the summing network. The above equations are true for ideal rise and fall times of the square wave. When the rise and fall times are non - zero, the audio output signal has distortion that is a function of the percentage of modulation and the ratio of the sum of the rise and fall times to the period of the square wave. Using a trapezoidal approximation and a Fortran IV program shown after the distortion equations, the amplitude distortion of the audio signal is calculated for

various sawtooth frequencies, sum of rise and fall times, and percentage of modulation.



Percentage of modulation = m

Minimum area $((1-m)\ T/2 - (t_r + t_f)/2)\ 2V$

Ideal minimum area = $(1-m)\ TV$

Maximum area = $((1+m)\ T/2 - (t_r + t_f)/2)\ 2V$

Ideal maximum area = $(1+m)\ TV$

Middle point area = $(T/2 - (t_r + t_f)/2)\ 2V$

Ideal middle point area = TV

$$\text{Error in minimum area} = \frac{(t_r + t_f)}{(1-m)\ T}$$

$$\text{Error in maximum area} = \frac{(t_r + t_f)}{(1 + m)\ T}$$

$$\text{Error in middle area} = \frac{(t_r + t_f)}{T}$$

$$\text{V audio} = \frac{m\ (2V)}{2}\ ,\ \text{Distortion} = \frac{\text{Error Min.} - \text{Error Max.}}{2}$$

```
$1BFTC ERROR    M94/2, XR7, NODECK

      1 FORMAT (12H1FREQUENCY =, F11.4, 3H KC,  3X, 13HTIME
       1PERIOD =  F11.4,  13H MICROSECONDS, 3X, 28HSUM OF RISE
       2AND FALL TIMES =, F11.4, 12H NANO SECONDS)

      4 FORMAT (22H-PERCENT OF MODULATION, 3X, 21HERROR OF
       1MINIMUM AREA, 4X, 20 HERROR OF MIDDLE AREA, 5X, 21
       2HERROR OF MAXIMUM AREA, 4X, 17HOUTPUT DISTORTION/
        32X, 4(7HPERCENT, 18X)/)

      2 FORMAT (5X, 4(F11.5, 14X), F11.5)

        DO 3 I = 1, 19

        DO 3 J = 1, 50

        TI = I - 1

        T = 1. + .5 * TI

        F = (1.E + 3)/T

        ST = 10 * J

        WRITE (6, 1) F, T, ST

        WRITE (6, 4)

        DO 3 K = 1, 20

        XM = (K - 1) *5

        X = 10. *ST/T

        EMIN = X/(100. - XM)

        EMID = X/100.

        EMAX = X/(100. +XM)

        EOUT = (EMIN-EMAX)/2.

      3 WRITE (6, 2) XM, EMIN,  EMID, EMAX, EOUT

        CALL EXIT
        STOP
        END
```

Figures 8 and 9 show the audio distortion versus the percentage of modulation for different sums of the rise and fall times for a square wave frequency of 200 KC.

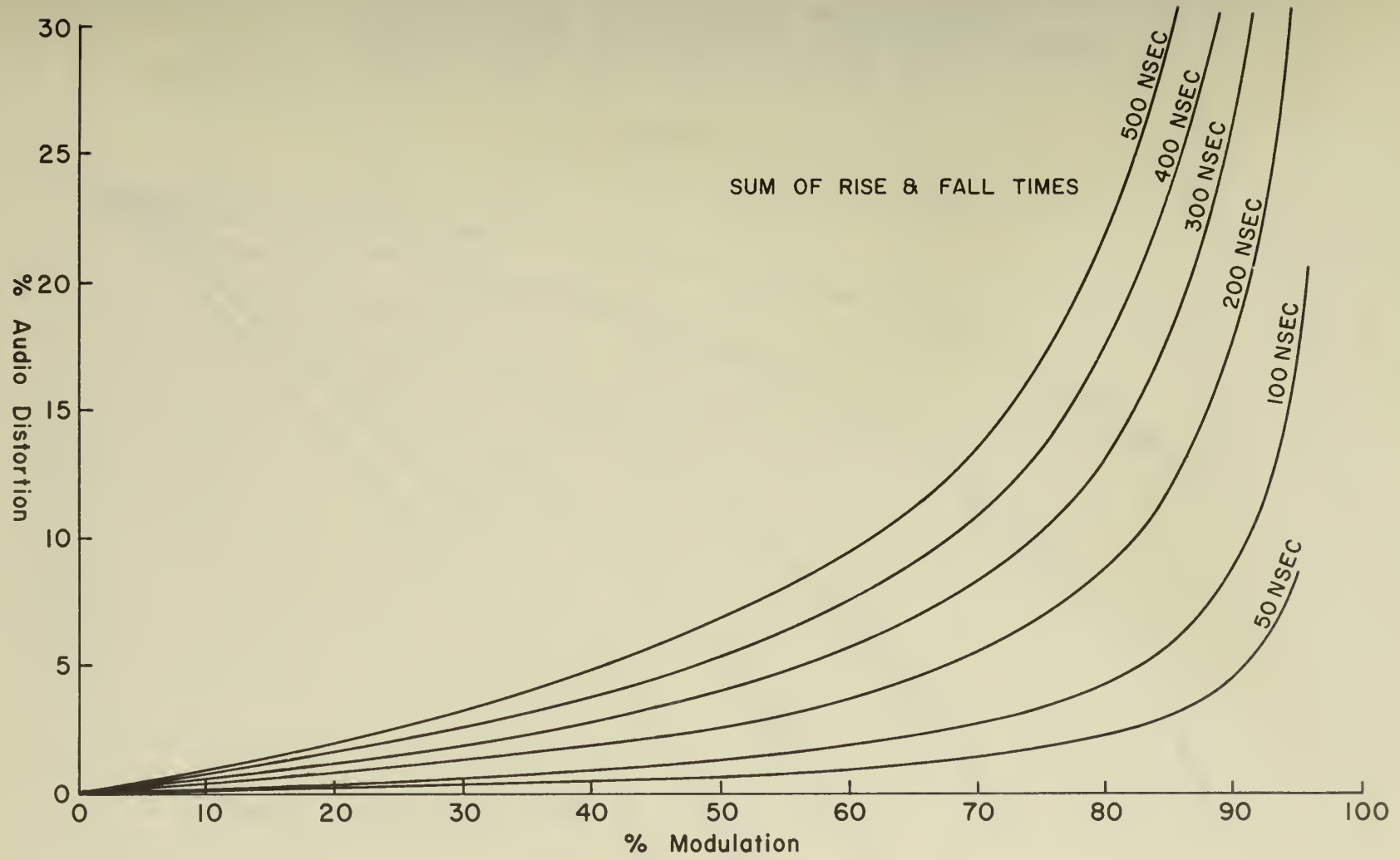


FIGURE 8. AUDIO SIGNAL DISTORTION DUE TO THE FINITE RISE & FALL TIMES OF THE EDGE MODULATED SQUARE WAVE VERSUS PERCENTAGE MODULATION

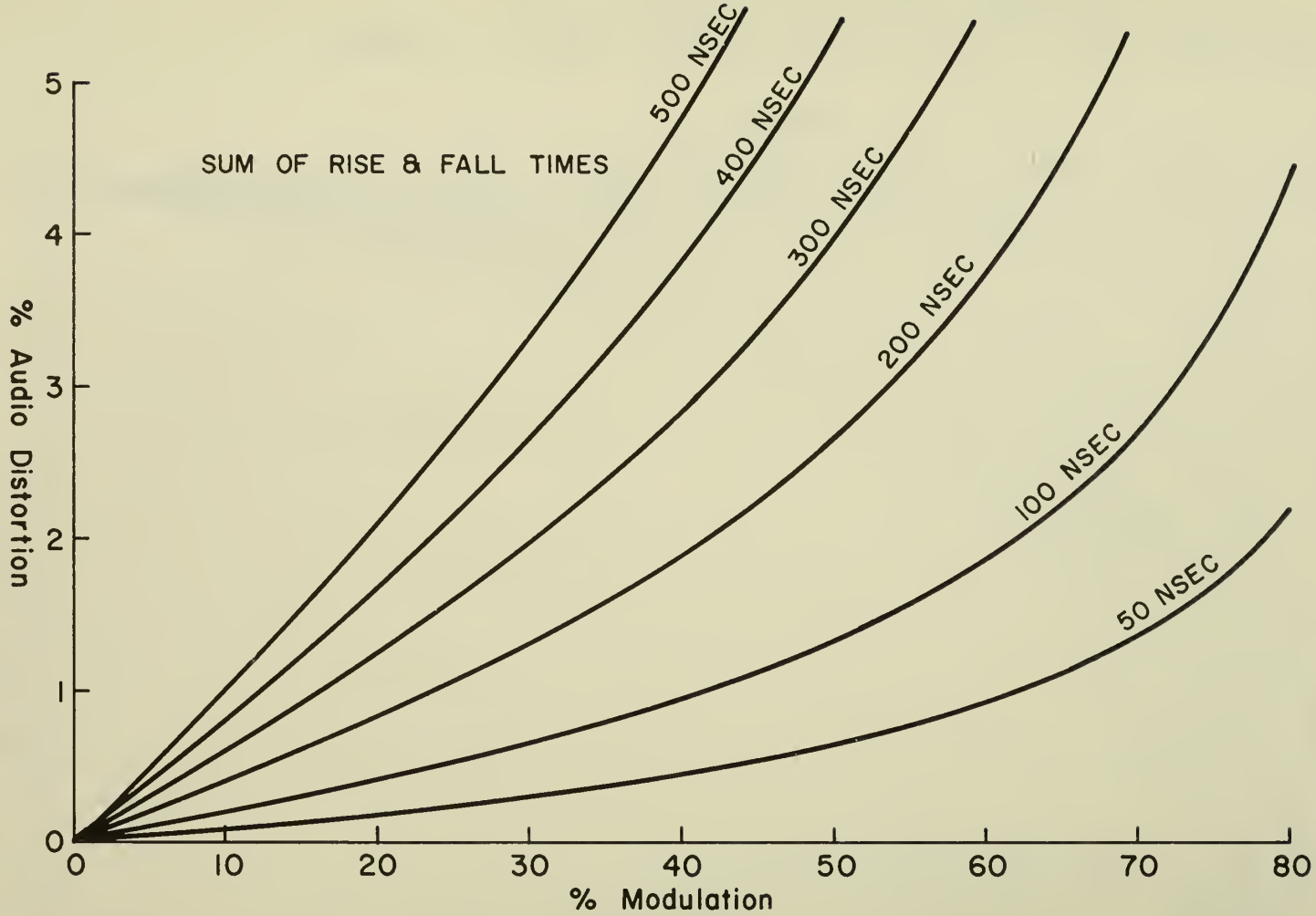


FIGURE 9. AUDIO SIGNAL DISTORTION DUE TO THE FINITE RISE & FALL TIMES OF THE EDGE MODULATED SQUARE WAVE VERSUS PERCENTAGE MODULATION

3. EXPERIMENTAL RESULTS

The comparison between the designed and the actual sawtooth generator is shown in Table 1.

TABLE 1

Item	Calculated	Measured
$V_{out_{p-p}}$	6.0 volt	4.85 volt
% of Modulation	80%	75%
Current Source Resistor	2,320 ohm	3,308 ohm
Nonlinearity of Ramp	0	$\pm$.6%
Slope of Ramp	$1.33 \times 10^{+6}$ volt/sec.	$.933 \times 10^{+6}$ volt/sec

The actual sawtooth generator's output is shown in Figure 10.

The sawtooth signal at the output of the summing network allows for 2.15 volt modulation or 75% modulation with $\pm$1.67% error in linearity. For 75% modulation, an audio signal of 3.5 volt peak-to-peak is applied at the audio input which has an ac input impedance of 3,000 ohm. The sawtooth signal at the output of the summing network is shown in Figure 11.

The rise and fall times of the power amplifier output are improved by matching the output transistors and inserting the 240 picofarad capacitor between the collectors of the first-stage transistors of the power amplifier. Program SSNA was used to select the capacitor's value. The resulting rise time is 86 nanosecond , and the resulting fall

time is 136 nanosecond when the amplifier is loaded with a 15 ohm resistor. When the amplifier is loaded with the low pass filter, the rise and fall times are respectively 786 and 640 nanosecond. The poor quality in the rise and fall times, with the filter as the load, is due to the large capacitive content in the filter's input impedance. If a loudspeaker is used, which has an inductive component in the input impedance, the rise and fall times are not affected as they are with the low pass filter.

The comparison between the calculated gain and phase and the measured gain and phase for the low-pass filter is shown in Figure 12.

The comparison between resistive loading and filter loading on the power amplifier output for dc signal input at the audio input is shown in Figure 13.

The amplifier and filter voltage gain versus frequency and percent modulation is shown in Figure 14. Note, the data for Figure 14 was taken with the poor rise and fall times. Even with the poor rise and fall times, the pahse shift due to the amplifier (subtracting the filter shift from the overall phase shift) is 4^{o} at 47 KC.

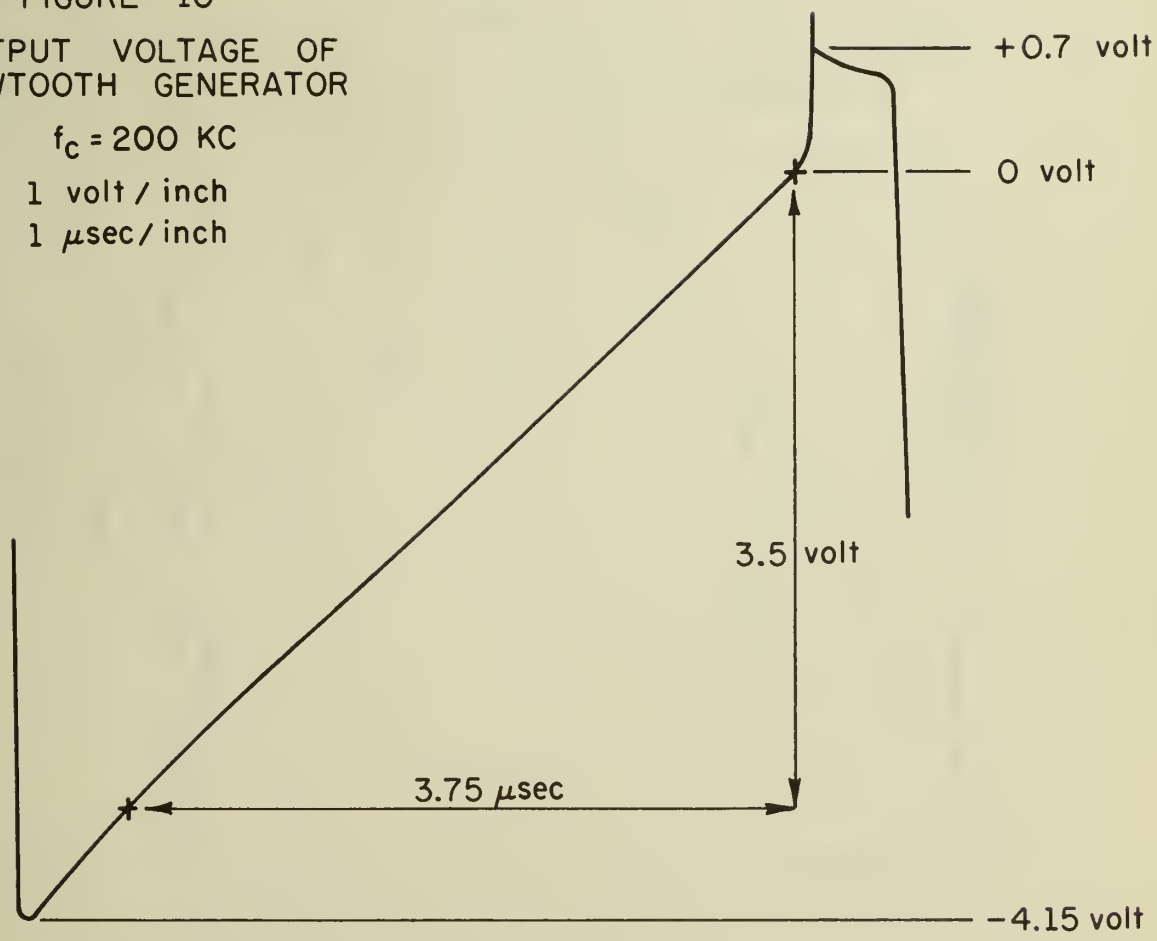
FIGURE 10

OUTPUT VOLTAGE OF SAWTOOTH GENERATOR

f_c = 200 KC

1 volt / inch

1 μsec / inch



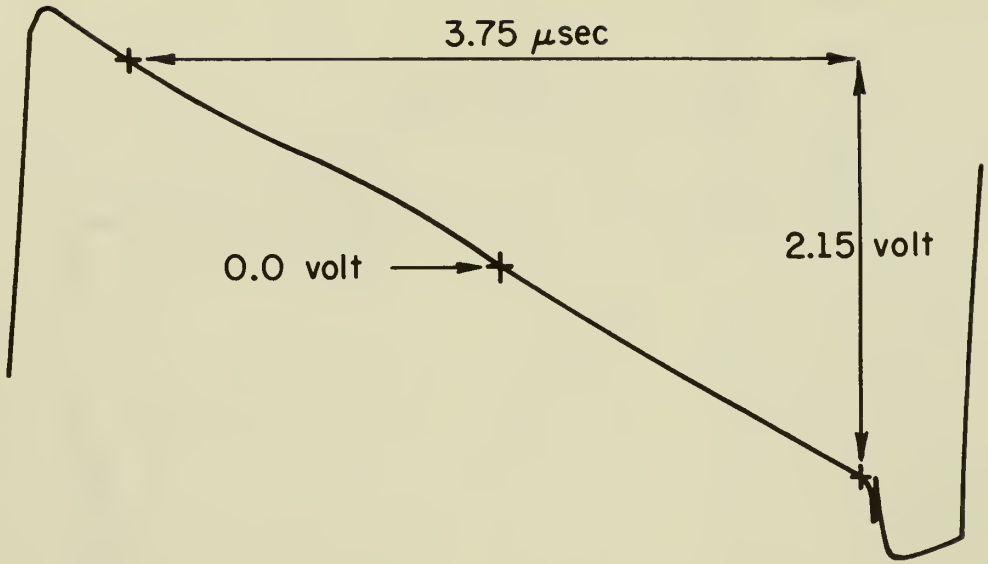


FIGURE 11

SUMMING NETWORK OUTPUT
LOADED WITH DIODE NETWORK ONLY
NO AUDIO SIGNAL
75% MAXIMUM MODULATION
1 volt/inch
1 μsec/inch

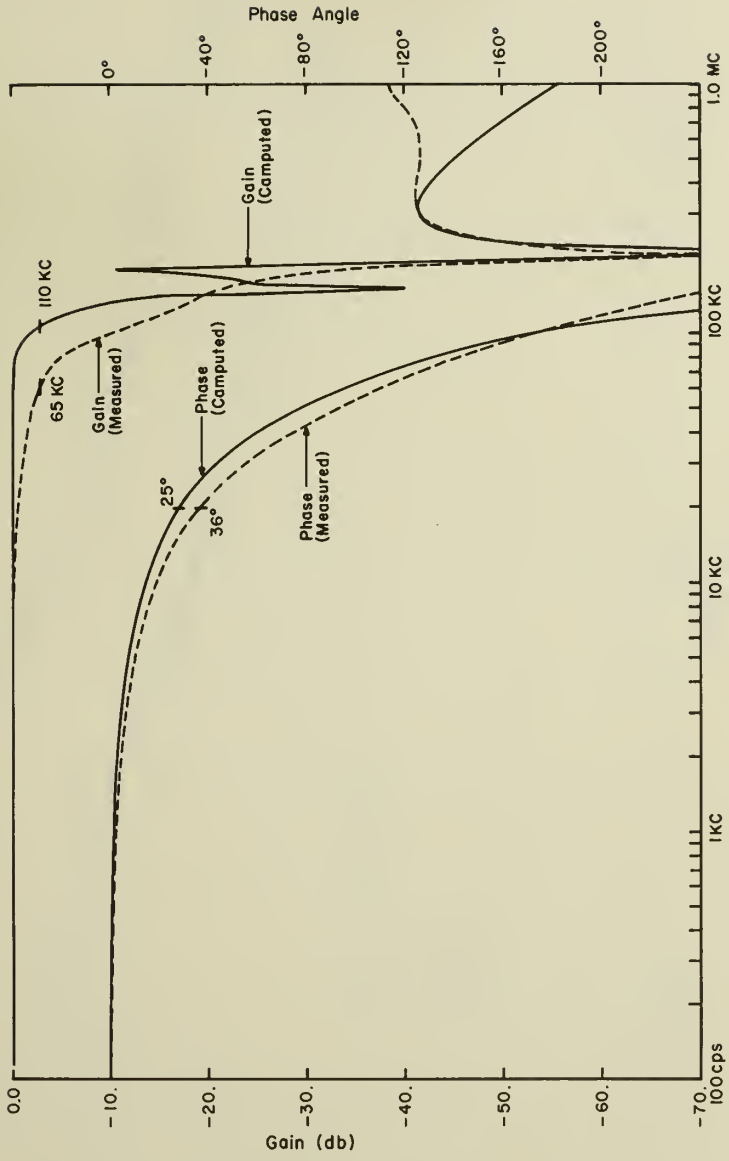


FIGURE 12. COMPARISON BETWEEN COMPUTED & MEASURED FILTER RESPONSE

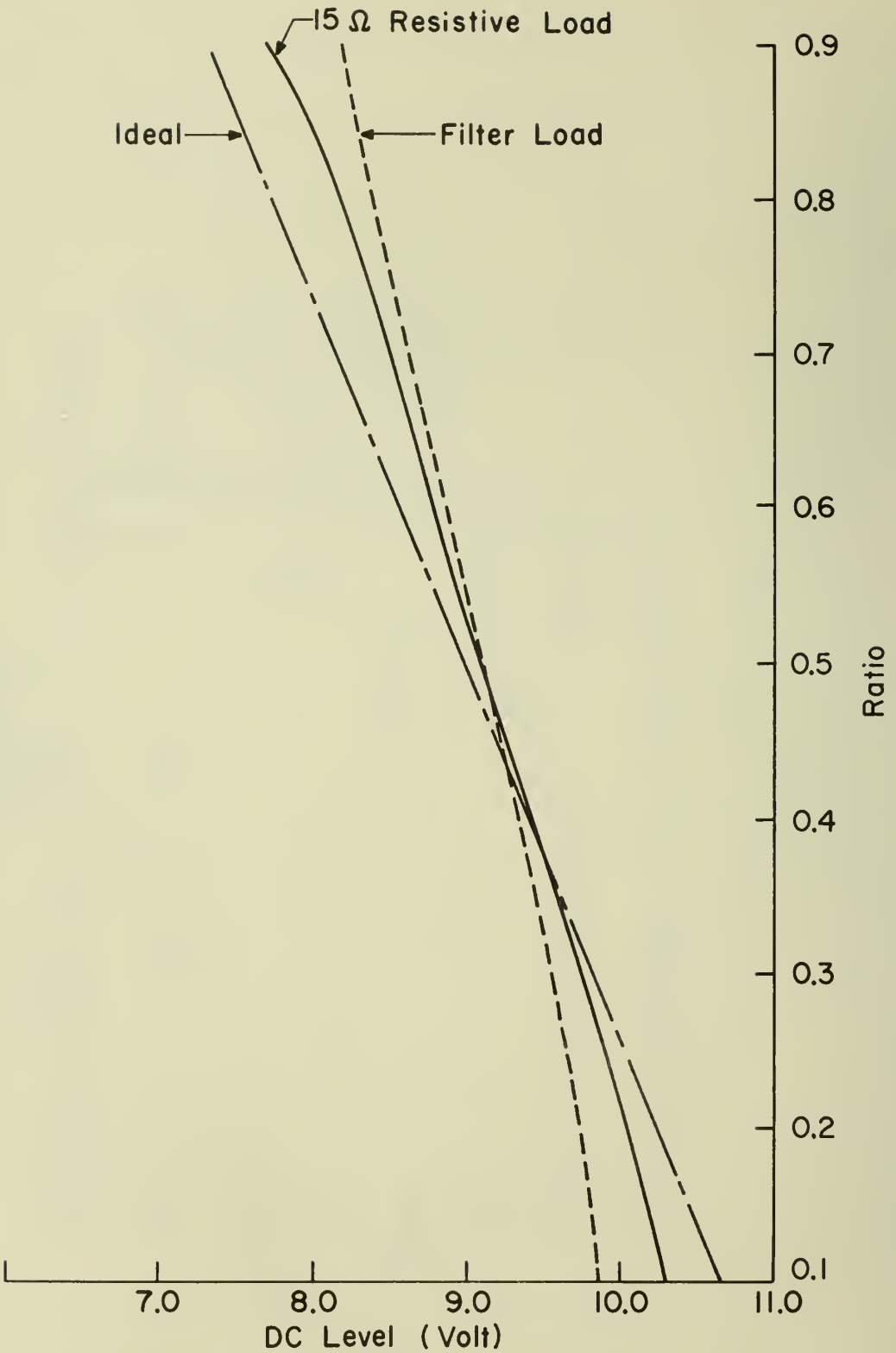


FIGURE 13. RATIO OF DOWN LEVEL TO TOTAL PERIOD OF OUTPUT MODULATED SQUAREWAVE VERSUS DC VOLTAGE AT AUDIO INPUT.

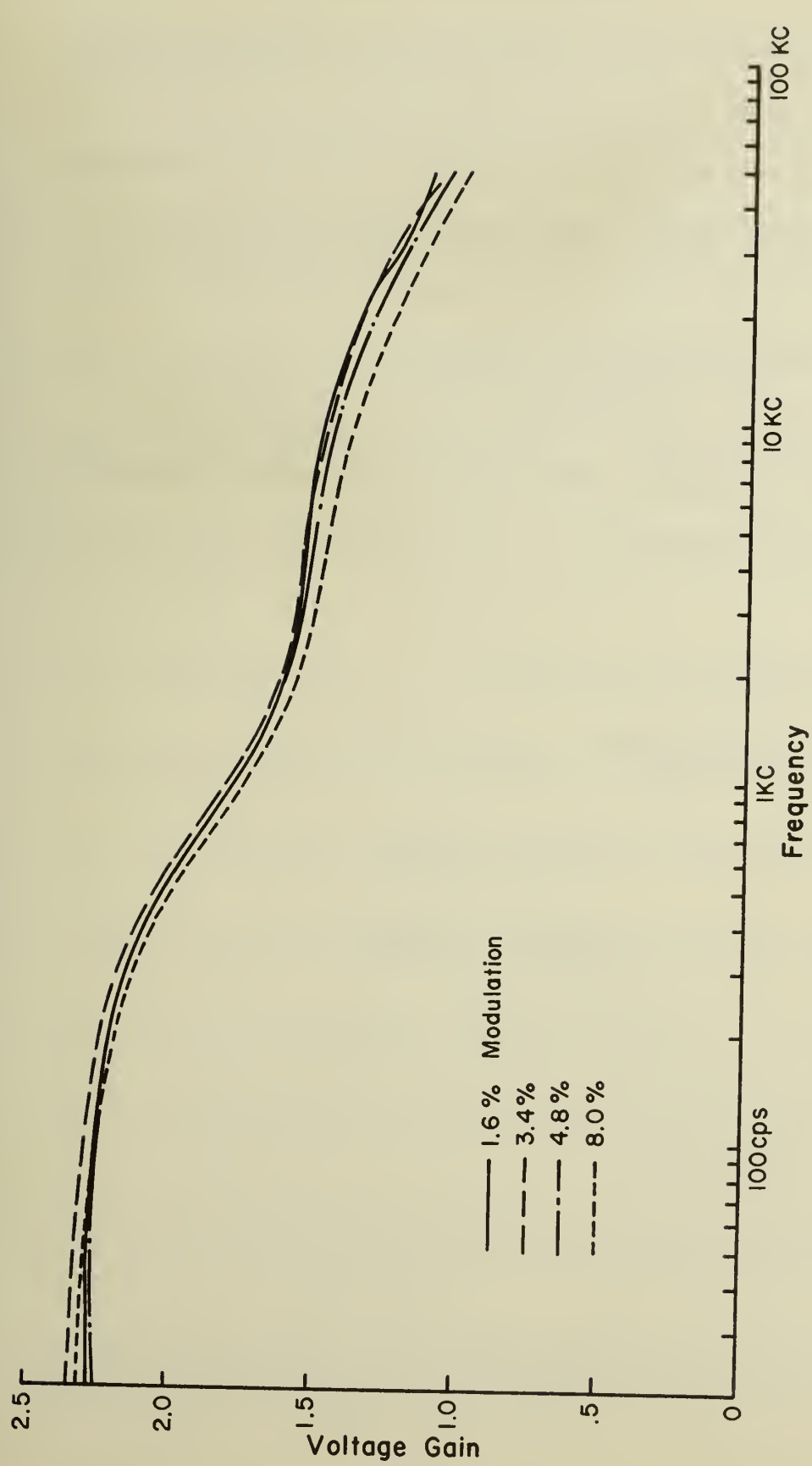


FIGURE 14. VOLTAGE GAIN OF COMPLETE AMPLIFIER AND FILTER

4. CONCLUSIONS

The only purpose for the low-pass filter is to prove the presence of the audio signal whose amplitude is the percentage of modulation times one half the square wave amplitude. Using a loudspeaker as the load, the rise and fall times of the amplifier output square wave are similar to the rise and fall times of the amplifier output square wave when the amplifier is loaded with a resistive load. The model used had only 25 db power gain. By increasing the power supply voltages and adjusting the resistors in the power amplifier, the power gain is increased.

Example:

1 watt output transistors (germanium)

$$I_{CON} = \frac{\text{Power of Transistor}}{2 \times V_{CE_{SAT}}} = \frac{1}{2(.3)} = 1.667 \text{ ampere}$$

$$R_o = 15\Omega, \pm V \text{ (supply)} = R_o I_{CON} + V_{CE_{SAT}} = 25.3 \text{ volt}$$

$$\text{Maximum Power gain} = 10 \log \left[\frac{(25)^2}{15} \times \frac{3,000}{(3.5)^2} \right]$$

$$= 10 \log (1.0204 \times 10^4) = 40 \text{ db}$$

Maximum Power in speaker is 41.66 watt as compared to 7.4 watt output for class B push pull.

5. LIST OF REFERENCES

1. Modulation Theory by Harold S. Black, D. Van Nostrand Company, Inc., New York, 1953, pp. 263-280.

2. "A Two-State Modulation Simplifies Audio Circuits" by A. G. Bose, Electronics, August 23, 1963, pp. 36 and 38.

3. "A Two-State Modulation System" by A. G. Bose, Quarterly Progress Report #70, MIT Research Laboratory of Electronics, July 15, 1963, pp. 198-205.

4. "A Two-State Modulation System" by A. G. Bose, paper #7.1 of the Western Electronics Show and Convention, 1963.

5. Linear Amplifier Design Manual by R. J. Bymes, Standards Engineering, General Products Division, IBM, April 1963.

6. Communication Engineering by W. L. Everitt and G. E. Anner, Second Edition, 1937, McGraw-Hill Company, Inc., New York, pp. 179-214.

7. Introduction to Fortran by S. C. Plumb, McGraw-Hill Company, Inc. New York, 1964.

8. Functional Circuits and Oscillators by Herbert J. Reich, D. Van Nostrand Company, Inc. 1961, pp. 220-236.

9. "Junction Transistor Circuits Application" by P. G. Salzer, Electronics, August, 1953, page 173.

10. Introduction to Modern Network Synthesis by M. E. Van Valkenburg, John Wiley & Sons, Inc., 1960, pp. 470-482.

11. Communication Circuits by L. A. Ware and H. R. Reed, Third Edition, 1962, John Wiley & Sons, Inc. New York, pp. 146-205.

12. General Electric Transistor Manual, Sixth Edition, 1962, pp. 130-138 and p. 169.

13. IBM 7090/7094 Programming Systems, Fortran IV Language, IBM Systems Reference Library, File Number 7090-25, Form Number C28-6274-3, November 1964.

14. IBM 7090/7094 IBSYS Operating System, Version 13, IBJOB Processor, IBM System Reference Library, File Number 7090-27, Form Number C28-6389-1, July 1965.

17. IBM 7090/7040 Direct Couple Operating System Programmer's Guide, IBM Systems Reference Library, File Number 7090-36, Form Number C28-6382-3, March 1965.

APPENDIX A

Circuit Design and Analysis Programs

ASAP

Automated Statistical Analysis Program description below was written by Arthur G. Kennard.

"ASAP is an 'Automated Statistical Analysis Program' that was developed for the IBM 7090/94 computer. This program is designed to perform a Monte Carlo statistical analysis on the d-c currents and voltages of transistor and diode circuits. The mathematical d-c model for such a transistor-diode circuit is a set of equations, formulated using the simple rules of algebra. Such a set of algebraic simultaneous equations will always have a unique solution for a given biasing condition. Moreover, such a solution can always be obtained by successive or step-by-step elimination of the unknowns. The task of generating these equations and the mechanics of obtaining the solutions become difficult and error prone, especially when the number of circuit components becomes large, particularly those that are nonlinear such as transistors and diodes. This task becomes almost impossible if one has to analyze circuits with extensive feedback loops.

"A high-speed scientific computer can perform the mechanics and produce the solution faster, more economically, and more reliably. However, a computer always requires a well-defined algorithm capable of handling a general case.

"This project was intended to investigate and establish such an algorithm for a general transistor and diode d-c circuit analysis. It was intended that the user will be required only to provide a simple topological description of the circuit in an English-text form, thus eliminating the need for writing the d-c equations manually. The ASAP program, through a pattern recognition program, SHADOW, scans and analyzes this input data, producing a table which indicates the sections or subpatterns of this data. ASAP uses this data to write the set of Kirchoff equations, then solves them algebraically using the Gauss reduction method. The program then writes a complete source program subroutine (using FORTRAN programming language), compiles this subroutine to convert it into machine language, and then calls on another subroutine which will perform the statistical analysis of the circuit. This process is carried out automatically from start to finish, thus justifying the name 'Automated Statistical Analysis Program - ASAP.'

"The unique feature of this method is that the equation solution is carried out analytically (symbolically) in almost the same manner as it would be done by hand. In essence, these equations are solved once analytically, rather than many thousands of times if one is required to perform a statistical simulation of a circuit.

"The topological description of the circuit may include resistors, voltage sources, current sources, diodes, and transistors. The diodes and transistors are represented by voltage-current tables supplied as input data. All items of the topolotical description must include the appropriate tolerances, and density functions. The output information is always given in tabular form. A frequency plot is given when requested.

"A feature of this program is the ability to determine the effects of component variation on the output parameters. The program computes two types of sensitivity. The first, statistical sensitivity, is a qualitative analysis where the measure of the spread of each parameter about the mean value is taken into consideration. The second type is based on a 1% deviation of each component parameter from its nominal value.

"A requirement for such a system is that it must perform a statistical analysis of the circuit. The most widely known and accepted method is the Monte Carlo simulation process, since it makes no assumptions about the statistical nature of any component parameter distribution but will accept any continuous density function.

"Briefly stated, the Monte Carlo method of treating system analysis is a scheme by which the performance of a large number of simulated samples of a system can be evaluated when the system is comprised of elements with values that may vary between tolerance limits. By repeatedly selecting random combinations of these parameters and computing the variables of the system, a valuable indication of the system's probability of meeting specific performance criteria can be derived.

"The Monte Carlo sampling process is analogous to providing a large sample of every component in the circuit. The samples are chosen so that they will have the statistical characteristics of their population. From each component-sample set, select one element, build the circuit in such a way that no new random variables are introduced in the process, and measure and record the dependent parameters of the circuit with caution. This operation is repeated many times. The dependent variables are then tabulated in a statistical frequency distribution. The subroutine that will perform the statistical analysis is called STRESS (Statistical Reliability Evaluation by Synthetic Sampling).

"The ASAP program is composed of two parts. The first is also called ASAP and is designed and programmed to accept the user's simple topological description of his circuit, and the component parameter information, such as their nominal values, the tolerances and the type of density function that characterizes each component. The output of this program is another computer program which contains all the statistical information and mathematical models of the circuit and its nonlinear components. The second part of this program, STRESS, performs the statistical analysis.

"This implies that one can, by making the necessary modifications, eliminate the STRESS capability and replace it by any other design criteria whether it be Taylor design, nominal design, or any feasible combination. It is not difficult for the user to convince himself that these design criteria are but special cases of the statistical design. For example: ASAP, as it stands, can produce the worst-case circuit analysis, by setting all component parameters at their worst-case tolerance limits and with zero tolerance about these selected values. Thus, the random-number generator will always select these worst-case limits to be used in the analysis. Similarly, the nominal design can be accomplished by setting all component parameters at their specified nominal value and with zero tolerance about these values."

ACOP

Automated Circuit Optimum Program uses the first part of ASAP. The user defines the topology of the circuit and specifies the values or range of values for the circuit parameters. The program does the nominal case and tolerance case if tolerances are specified. The user defines a variable expressed in terms of input and output parameters. The second part of the program uses the Monte Carlo simulation process of selecting nominal circuit components and calculates the above defined variable. After doing the specified number of random selections, the program selects the minimum value of the optimum variable and then does a direct search on the component values to find the true minimum of the optimum variable. Then the component tolerances are included and

the program will minimize the optimum variable again. This program was written by Arthur G. Kennard (author of ASAP).

SSNA

The Steady-State AC Network Analysis Program (SSNA) is developed for an IBM 7094 model 2 computer. The program analyzes linear networks in the small signal sinusoidal frequency domain. The network can consist of:

1. Constant lump parameters: resistors, capacitors, and inductors
2. Distributive transmission lines or distributive monolithic resistors
3. Transistors (the program has two transistor models of which the data for either can be entered on one data card for each transistor)

The program allows for one resistance, one inductance, one capacitance, and/or Q of coil to be entered on one data card (passive data branch). A configuration number defines how these R, L, and/or C are connected together to form a two terminal network. There can be up to three of these R, L, and C configurations connected in any series-parallel combination, as long as the overall combination (a branch set) is a two terminal network. These two external terminals then become two major nodes.

Circuit Limitations:

Resistors	633
Inductors	633
Capacitors	633
Transmission Lines	20
Transistors	10
Nodes	1708
Major Nodes	20

The program generates its own equations from a topological description of the network. The network data is in fixed format, but no programming experience is needed.

There are four general modes of operations (which can be done individually or all at once with the network data entered only once):

1. Frequency response (on the log or linear scale).
2. Variation of any passive parameters by incrementing the parameter with a frequency response for each increment.
3. Variation of any passive branch set by direct substitution with a frequency response for each modification.
4. Variation of any transistor's parameters by substitution with a frequency response for each substitution.

The number of frequency points a given network can be solved for is unlimited. Any number of networks described with previously stated components can be cascaded together.

The output results for single-ended networks may consist of:

1. Node voltages
2. One of sixteen possible transfer functions between any two major nodes
3. Input impedance (one of three functions)
4. Output impedance (one of four functions)
5. Mutual impedance (impedance between the input and the output nodes)
6. Semilog plot of the transfer function
7. Nyquist plot of the transfer function
8. Printer plots of the three impedance functions
9. When cascading, 2, 6, and 7 outputs are also available for the accumulative networks.

The output results for differential networks may consist of:

1. Voltage gains for both sides of the network
2. Differential voltage gain
3. Common mode rejection
4. Common mode rejection ratio
5. Delta and wye equivalent input impedances
6. Nyquist and semilog plots of the above voltage gains
7. Semilog plot of the common mode rejection ratio

8. Rectangular plots of the equivalent input impedances
9. When cascading, the above outputs are available for the accumulative network

SSNA will load in 50 second and will analyze 1899 component network in 2.4 second per frequency point.

Programs ASAP, ACOP, and SSNA are IBM experimental programs and are not available for general public use.

APPENDIX B

Samples of Computer Runs

The minimum open loop gain of the sawtooth generator to insure the oscillator operation with worse-case components using SSNA shown on pages 47 to 48.

Selecting the ac emitter resistor of the second transistor in the impedance transformer using SSNA shown on pages 49 to 50.

The dc designing of the summing network using ACOP shown on pages 51 to 56.

The dc analysis of the summing network using ASAP shown on pages 57 to 60.

The ac analysis of the low pass filter using SSNA on pages 61 to 64.

MINIMUM OPEN LOOP GAIN

RESISTANCE	INDUCTANCE	CAPACITANCE	Q OF COIL	N	NODE TO NODE	OPERATOR
6.75KOHM	-0. H	-0. F	-0.	1	1 -0	
-0. OHM	-0. H	90.00 PF	-0.	8	1 2	
351.00 OHM	-0. H	-0. F	-0.	1	2 -0	
351.00 OHM	-0. H	-0. F	-0.	1	6 -0	
100.00 OHM	-0. H	2.00 PF	-0.	1	3 -0	
-0. OHM	-0. H	1.62 NF	-0.	8	6 8	
100.00 OHM	-0. H	2.00 PF	-0.	1	7 -0	
5.17KOHM	-0. H	-0. F	-0.	1	4 -0	PARALLEL
5.17KOHM	-0. H	-0. F	-0.	1	4 -0	
2.37KOHM	-0. H	-0. F	-0.	1	5 -0	
-0. OHM	-0. H	-0. F	-0.	-1	-0 -0	

TRANSISTOR PARAMETERS FOR TX 1 BASE 9 COLLECTOR 2 EMITTER 3

CC = 2.50 PF FT = 212.00 MC HFE = 45.00 HIE = 850.00 OHM
RBB = 42.00 OHM CCB = 2.00 PF CCE = 0.63 PF CBE = 1.20 PF

TRANSISTOR PARAMETERS FOR TX2 BASE 1 COLLECTOR 6 EMITTER 7

CC = 3.30 PF FT = 209.00 MC HFE = 39.00 HIE = 650.00 OHM
RBB = 36.00 OHM CCB = 2.10 PF CCE = 0.68 PF CBE = 1.70 PF

TRANSISTOR PARAMETERS FOR TX3 BASE 4 COLLECTOR 8 EMITTER 5

CC = 2.36 PF FT = 229.00 MC HFE = 71.00 HIE = 1.15 KOHM
RBB = 95.50 OHM CCB = 1.60 PF CCE = 0.60 PF CBE = 0.65 PF

GAIN BETWEEN NODE 9 AND NODE 8

FREQUENCY CPS	IND. NETWORK GAIN GAIN	PHASE
1.000 CPS	1.322E-05	90.0
2.000 CPS	2.643E-05	90.0
4.000 CPS	5.287E-05	90.0
8.000 CPS	1.057E-04	90.0
10.000 CPS	1.322E-04	90.0
20.000 CPS	2.643E-04	90.0
40.000 CPS	5.287E-04	90.0
80.000 CPS	1.057E-03	90.0
100.000 CPS	1.322E-03	90.0
200.000 CPS	2.643E-03	90.0
400.000 CPS	5.287E-03	89.9
800.000 CPS	1.057E-02	89.9
1.000 KCPS	1.322E-02	89.9
2.000 KC	2.643E-02	89.7
4.000 KC	5.286E-02	89.5
8.000 KC	0.106	89.0
10.000 KC	0.132	88.7
20.000 KC	0.264	87.4
40.000 KC	0.527	84.8
80.000 KC	1.041	79.6
100.000 KC	1.291	77.1
200.000 KC	2.421	65.2
400.000 KC	3.974	46.5
800.000 KC	5.228	25.2
1.000 MC	5.468	18.9
2.000 MC	5.796	1.7
4.000 MC	5.671	-15.2
8.000 MC	5.014	-36.4
10.000 MC	4.664	-44.5
20.000 MC	3.310	-73.6
40.000 MC	2.019	-109.6
80.000 MC	1.183	-157.2
100.000 MC	1.016	-176.0
200.000 MC	0.711	118.5
400.000 MC	0.567	60.7
800.000 MC	0.484	26.5
1.000 GC	0.466	19.8
2.000 GC	0.427	7.6

THESIS VOLTAGE FEEDBACK PAIR 10/25/66

RESISTANCE	INDUCTANCE	CAPACITANCE	Q OF COIL	N	NODE TO NODE	OPERATOR
-0.0 OHM	-0. H	1.80 NF	-0	8	1	-0
1.20KOHM	-0. H	-0. F	-0	1	2	-0
10.00 OHM	-0. H	-0. F	-0	1	3	-0
1.10KOHM	-0. H	-0. F	-0	1	4	-0
5.60KOHM	-0. H	100.000 NF	-0	8	-0	-0

TRANSISTOR PARAMETERS FOR TX1 BASE 1 COLLECTOR 2 EMITTER 4

CC = 2.30 PF FT = 226.00 MC HFE = 66.00 HIE = 1.05 KOHM
RBB = 48.00 OHM CCB = 2.20 PF CCE = 0.69 PF CBE= 1.00 PF

TRANSISTOR PARAMETERS FOR TX2 BASE 2 COLLECTOR 4 EMITTER 3

CC = 1.00 PF FT - 229.00 MC HFE - 69.00 HIE = 1.20 KOHM
RBB = 180.00 OHM CCB = 1.55 PF CCE = 0.59 PF CBE= 0.16 PF

VARYING PARAMETERS FOR BRANCH 1 OF THE BRANCH SET BETWEEN NODE 3 AND THE

REFERENCE NODE

RESISTANCE = 200.00 OHM
INDUCTANCE = -0. H
CAPACITANCE = -0. F
Q OF COIL = -0.

GAIN BETWEEN NODE 1 AND NODE 4

FREQUENCY CPS	IND. NETWORK GAIN GAIN	PHASE	INPUT IMPEDANCE REAL	IMAGINARY	OUTPUT IMPEDANCE REAL	IMAGINARY
100.000 KC	0.997	-0.0	135.61KOHM	-J 178.86KOHM	3.15 OHM	-J 2.16 OHM
150.000 KC	0.997	-0.0	75.73KOHM	-J 149.70KOHM	3.15 OHM	-J 1.41 OHM
200.000 KC	0.997	-0.0	46.78KOHM	-J 123.32KOHM	3.15 OHM	-J 1.03 OHM
250.000 KC	0.997	-0.0	31.35KOHM	-J 103.37KOHM	3.15 OHM	-J 788.76 LOHM
300.000 KC	0.997	-0.0	22.34KOHM	-J 88.43KOHM	3.15 OHM	-J 625.16 LOHM

TOPOLOGICAL INPUT DATA

NOVEMBER 30, 1966

5:08 PM

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2000 CASES
NO SENSITIVITIES
DONT VERIFY
INPUTS
R1, 1.0 TO 10.0, SHAPE1
R2, 0.5 TO 10.0, SHAPE1
R3, .025 TO 5.0, SHAPE1
R4, .1 TO 5.0, SHAPE1
R5, .1 TO 10., SHAPE1
R7, .1 TO 10.0, SHAPE1
R11, VA1-VB1, R1, VE21, TOL .05
R12, VA2-VB2, R1, VE22, TOL .05
R21, VB1-GND, R2, VE21, TOL .05
R22, VB2-GND, R2, VE22, TOL .05
R31, VP121-VE11, R3, VE21, TOL .05
R32, VP122-VE12, R3, VE22, TOL .05
R41, VC1-VM121, R4, VE21, TOL .05
R42, VC2-VM122, R4, VE22, TOL .05
R51, VE21-VM121, R5, VE21, TOL .05
R52, VE22-VM122, R5, VE22, TOL .05
R71, VE21-VB1, R7, VE21, TOL .05
R72, VE22-VB2, R7, VE22, TOL .05
VA1=9.9
VA2=8.1
VM121=-12.6
VM122=-11.4
VP121=11.4
VP122=12.6
T11,PNP,VB1,VC1,VE11,CURVE 1,BETA1=30 TO 150
T12,PNP,VB2,VC2,VE12,CURVE 1,BETA2=30 TO 150
T21,NPN,VC1,VP121,VE21,CURVE 1,BETA21=30 TO 150
T22,NPN,VC2,VP122,VE22,CURVE 1,BETA22=30 TO 150
OUTPUTS
ZETA=0.,RANDOM,DIRECT
```

```
VBE1=VB1-VE11
VBE2=VB2-VE12
VBE21=VC1-VE21
VBE22=VC2-VE22
IR11
IR12
IR21
IR22
IR31
IR32
IR41
IR42
IR51
IR52
IR71
IR72
VB1
VB2
VC1
VC2
VE11
VE12
VE21
VE22
CURVE 1   DONT PLOT
          -.001,-1.,-1.,   0.,0.,0.,   .002,.56,.611,   .015,.61,.67,
0.32,.63,.69   .080,.66,.72,   .145,.67,.73,   .4,.69,.75,
.8,.71,.77,   1.7,.73,.79,   2.9,.75,.81,   4.0,.76,.82,
6.3,.77,.83,   11.8,.79,.85,   16.3,.80,.86
      END
```

DETERMINATION OF STARTING VALUES BY MONTE CARLO RANDOM SELECTION

FUNCTION ZETA = 4.8562410E 10 CASE 1

R1 = 4.3837602 R2 = 6.1011393 R3 = 1.4541998 R4 = 3.4852126 R5 = 6.4555717
R7 = 2.0716547

FUNCTION ZETA = 4.1314416E 10 CASE 3

R1 = 7.5089527 R2 = 7.2261320 R3 = 3.2178183 R4 = 4.9833114 R5 = 6.2858439
R7 = 2.1714134

FUNCTION ZETA = 3.5382809E 10 CASE 4

R1 = 4.1552201 R2 = 4.5355723 R3 = 4.8702351 R4 = 0.8417151 R5 = 0.1800920
R7 = 0.2711737

FUNCTION ZETA = 3.4205612E 10 CASE 7

R1 = 7.2622522 R2 = 5.6637523 R3 = 3.3130067 R4 = 4.7929067 R5 = 1.2528664
R7 = 4.0906226

FUNCTION ZETA = 2.6825306E 10 CASE 8

R1 = 5.1882831 R2 = 2.1768311 R3 = 4.6018390 R4 = 3.4709587 R5 = 7.6162526
R7 = 3.9064464

FUNCTION ZETA = 1.3451205E 09 CASE 15

R1 = 4.3471512 R2 = 5.8061206 R3 = 2.5730406 R4 = 2.8413317 R5 = 4.2616200
R7 = 5.8655604

FUNCTION ZETA = 1681229.4 CASE 62

R1 = 3.5500923 R2 = 8.0382104 R3 = 1.7880315 R4 = 1.0250802 R5 = 1.0182921
R7 = 9.2274735

FUNCTION ZETA = 1301776.3 CASE 91

R1 = 6.1998148 R2 = 5.7952254 R3 = 1.8937194 R4 = 1.2828325 R5 = 2.2963898
R7 = 8.6223669

FUNCTION ZETA = 610788.06 CASE 93

R1 = 2.6849269 R2 = 5.5272003 R3 = 2.0964828 R4 = 3.1921733 R5 = 3.8252712
R7 = 9.0438234

PARAMETER VALUES AFTER DIRECT SEARCH MINIMIZATION OF ZETA

R1 = 2.0382268 R2 = 6.4036058 R3 = 1.6143039 R4 = 2.6404109 R5 = 4.1318408
R7 = 7.5477084

OUTPUT PARAMETERS AFTER DIRECT SEARCH MINIMIZATION

PARAMETER	VALUE
ZETA	431528.80
VBE1	-0.7849149
VBE2	-0.7919883
VBE21	0.7354520
VBE22	0.7638962
IR11	2.1313836
IR12	1.4616797
IR21	0.8775557
IR22	0.8172704
IR31	3.4406490
IR32	4.4576544
IR41	3.3950524
IR42	4.3874085
IR51	2.0000536
IR52	2.6276523
IR71	-1.2916359
IR72	-0.6934011
VB1	5.3385447
VB2	4.9718034
VC1	-3.1874498
VC2	0.7637894

VE11	6.1234596
VE12	5.7637917
VE21	-3.9229018
VE22	-1.0673702E-04

TOPOLOGICAL INPUT DATA

NOVEMBER 30, 1966

12:57 AM

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10000 CASES
NO SENSITIVITIES
DONT VERIFY
INPUTS
R1, VA TO VB = 2.     , TOL .05
R2, VB TO GND = 6.2  , TOL .05
R3, VP12 TO VE1 = 1.6, TOL .05
R4, VC TO VM12 = 3.9 , TOL .05
R5, VE2 TO VM12 = 4.3 , TOL .05
R7, VE2 TO VB = 7.5 ,  TOL .05

VA=8.1 TO 9.9
VM12=-12.6 TO -11.4
VP12= 11.4 TO 12.6
T1, PNP, VB, VC, VE1, CURVE 1, BETA1=30 TO 150
T2, NPN, VC, VP12, VE2, CURVE 1, BETA2=30 TO 150
OUTPUTS
VBE1=VB-VE1, PLOT
VBE2=VC-VE2, PLOT
IR1, PLOT
IR2, PLOT
IR3, PLOT
IR4, PLOT
IR5, PLOT
IR7, PLOT
VB, PLOT
VC, PLOT
VE1, PLOT
VE2, PLOT
CURVE 1   PLOT
          -.001,-1.,-1.,   0.,0.,0.,   .002,.56,.611,   .015,.61,.67
.032,.63,.69,   .080,.66,.72,   .145,.67,.73   .4,.69,.75,
.8,.71,.77,   1.7,.73,.79,   2.9,.75,.81,   4.0,.76,.82,
6.3,.77,.83,   11.8,.79,.85,   16.3,.80,.86
      END
```

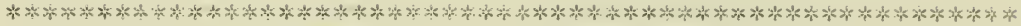
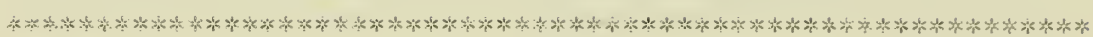
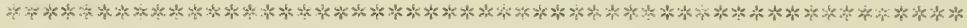
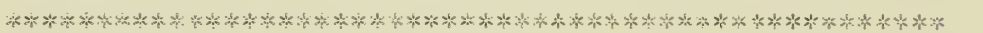
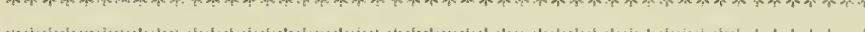
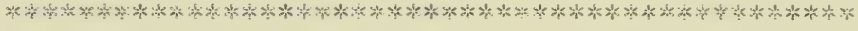
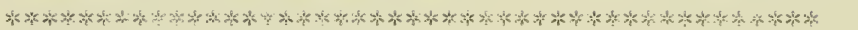
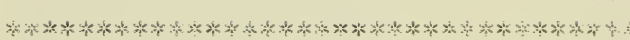
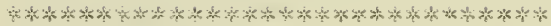
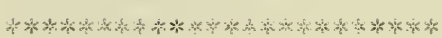
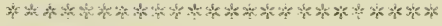
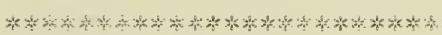
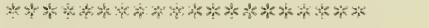
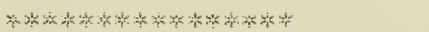
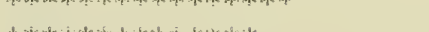
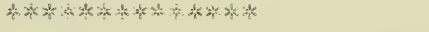
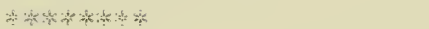
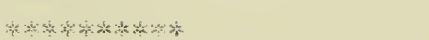
NOMINAL VALUE OF EACH OUTPUT PARAMETER (CALCULATED USING NOMINAL VALUE OF EACH INPUT PARAMETER)

VBE1	=	-0.784644
VBE2	=	0.767184
IR1	=	1.620232
IR2	=	0.928957
IR3	=	3.409887
IR4	=	3.349002
IR5	=	2.859052
IR7	=	-0.728749
VB	=	5.759536
VC	=	1.061106
VE1	=	6.544180
VE2	=	0.293922

DISTRIBUTION OF PERFORMANCE PARAMETER VE2 FOR 10000 CASES TESTED

MINIMUM= -2.634140 MEAN= 0.232330 MAXIMUM= 3.224456 NOMINAL= 0.293922 STD. DEV. = 0.929959

NO. CASES	CUMU-LATIVE DENSITY	PARA-METER VALUE	THE SCALE FACTOR FOR THE FOLLOWING ORDINATES IS 8
1	0.000	-2.63297	
3	0.000	-2.51345	
3	0.001	-2.39394	
12	0.002	-2.27442	**
14	0.003	-2.15491	**
13	0.005	-2.03539	**
31	0.008	-1.91588	****
38	0.011	-1.79636	*****
60	0.017	-1.67685	********
85	0.026	-1.55733	**********
122	0.038	-1.43781	**************
157	0.054	-1.31830	**********************
188	0.073	-1.19878	**************************
211	0.094	-1.07927	****************************
222	0.116	-0.95975	*****************************
282	0.144	-0.84024	************************************
315	0.176	-0.72072	**
360	0.212	-0.60121	**
396	0.251	-0.48169	**
416	0.293	-0.36218	**
445	0.337	-0.24266	**
453	0.383	-0.12315	**
499	0.433	-3.63037E-03	**
477	0.480	0.11588	**

NO. CASES	CUMU-LATIVE DENSITY	PARA-METER VALUE	
518	0.532	0.23540	
451	0.577	0.35492	
483	0.625	0.47443	
460	0.671	0.59395	
416	0.713	0.71346	
426	0.756	0.83298	
357	0.791	0.95249	
328	0.824	1.07201	
322	0.856	1.19152	
272	0.884	1.31104	
233	0.907	1.43055	
213	0.928	1.55007	
162	0.944	1.66958	
127	0.957	1.78910	
114	0.968	1.90862	
63	0.975	2.02813	
76	0.982	2.14765	
64	0.989	2.26716	
38	0.993	2.38668	
33	0.996	2.50619	
16	0.997	2.62571	
16	0.999	2.74522	
4	0.999	2.86474	
3	1.000	2.98425	
1	1.000	3.10377	
1	1.000	3.22328	

THESIS FILTER 12/2/66

RESISTANCE	INDUCTANCE	CAPACITANCE	Q OF COIL	N	NODE TO NODE	
60.00 LOHM	14.40 UH	75.00 NF	-0	1	1	2
100.00 LOHM	25.60 UH	-0. F	-0	1	2	3
50.00 LOHM	9.70 UH	56.00 NF	-0	1	3	4
40.00 LOHM	8.90 UH	68.00 NF	-0	1	4	5
-0. OHM	-0. H	100.00 NF	-0	8	2	-0
-0. OHM	-0. H	82.00 NF	-0	8	3	-0
-0. OHM	-0. H	62.00 NF	-0	8	4	-0
15.00 OHM	-0. H	-0. F	-0	1	-0	-0

INDIVIDUAL NETWORK VOLTAGE GAIN, V (OUT)/V (IN) FROM NODE 1 TO NODE 5 IN DB

V(OUT) DEFINED AS THE VOLTAGE AT THE OUTPUT NODE

V(IN) DEFINED AS THE VOLTAGE AT THE INPUT NODE

Z(IN) DEFINED AS THE IMPEDANCE SEEN AT THE INPUT NODE

Z(OUT) DEFINED AS THE IMPEDANCE SEEN AT THE OUTPUT NODE

INCLUDING ANY CASCADED LOAD

INDIVIDUAL NETWORK VOLTAGE GAIN, V(OUT)/V(IN) FROM NODE 1 TO NODE 5 IN DB

FREQUENCY CPS	IND. NETWORK GAIN GAIN	PHASE	INPUT IMPEDANCE REAL	IMAGINARY
1.000 CPS	-0.144	-0.0	15.25 OHM	J 17.78UOHM
2.000 CPS	-0.144	-0.0	15.25 OHM	J 35.55UOHM
4.000 CPS	-0.144	-0.0	15.25 OHM	J 71.11UOHM
8.000 CPS	-0.144	-0.0	15.25 OHM	J 142.22UOHM
10.000 CPS	-0.144	-0.0	15.25 OHM	J 177.77UOHM
20.000 CPS	-0.144	-0.0	15.25 OHM	J 355.54UOHM
40.000 CPS	-0.144	-0.1	15.25 OHM	J 711.08UOHM
80.000 CPS	-0.144	-0.1	15.25 OHM	J 1.42LOHM
100.000 CPS	-0.144	-0.1	15.25 OHM	J 1.78LOHM
200.000 CPS	-0.144	-0.3	15.25 OHM	J 3.56LOHM
400.000 CPS	-0.144	-0.6	15.25 OHM	J 7.11LOHM
800.000 CPS	-0.144	-1.1	15.25 OHM	J 14.23LOHM
1.000 KC	-0.143	-1.4	15.25 OHM	J 17.78LOHM
2.000 KC	-0.143	-2.8	15.25 OHM	J 35.62LOHM
4.000 KC	-0.142	-5.6	15.24 OHM	J 71.61LOHM
8.000 KC	-0.138	-11.2	15.23 OHM	J 146.25LOHM
10.000 KC	-0.136	-14.0	15.22 OHM	J 185.62LOHM
20.000 KC	-0.114	-28.2	15.13 OHM	J 416.60LOHM
40.000 KC	-6.453E-02	-57.9	14.86 OHM	J 1.16 OHM
80.000 KC	-0.351	-129.3	14.20 OHM	J 4.90 OHM
100.000 KC	-1.630	-176.9	14.08 OHM	J 9.99 OHM
200.000 KC	-54.08	-78.8	181.23LOHM	-J 38.48 OHM
400.000 KC	-42.44	-140.3	2.68LOHM	-J 10.47 OHM
800.000 KC	-51.74	-160.6	122.39UOHM	-J 4.77 OHM
1.000 MC	-55.34	-164.6	47.57UOHM	-J 3.78 OHM
2.000 MC	-67.02	-172.3	2.75UOHM	-J 1.87 OHM
4.000 MC	-78.98	-176.2	169.73NOHM	-J 929.43LOHM

FREQUENCY CPS	IND. NETWORK GAIN GAIN	PHASE	INPUT IMPEDANCE REAL	IMAGINARY
8.000 MC	-91.00	-178.1	14.90NOHM	-J 464.33LOHM
10.000 MC	-94.87	-178.5	5.59NOHM	-J 371.43LOHM
20.000 MC	-106.9	-179.2	-0. OHM	-J 185.69LOHM
40.000 MC	-118.9	-179.6	59.60NOHM	-J 92.84LOHM
80.000 MC	-131.0	-179.8	357.63NOHM	-J 46.42LOHM
100.000 MC	-134.9	-179.8	715.26NOHM	-J 37.14LOHM
200.000 MC	-146.9	-179.9	4.77UOHM	-J 18.57LOHM
400.000 MC	-158.9	-179.7	3.81UOHM	-J 9.28LOHM
800.000 MC	-171.0	-179.7	91.55UOHM	-J 4.64LOHM
1.000 GC	-174.0	-179.0	30.52UOHM	-J 3.71LOHM
2.000 GC	-186.9	-174.4	-183.11UOHM	-J 1.86LOHM

FREQUENCY CPS	IND. NETWORK GAIN GAIN	PHASE	INPUT IMPEDANCE REAL	IMAGINARY
100.000 KC	-1.630	-176.9	14.08 OHM	J 9.99 OHM
120.000 KC	-4.988	128.6	15.89 OHM	J 21.55 OHM
140.000 KC	-12.09	51.7	20.49 OHM	J 62.30 OHM
160.000 KC	-26.28	136.9	12.28 OHM	-J 175.67 OHM
180.000 KC	-15.18	84.0	6.34 OHM	-J 47.58 OHM
200.000 KC	-54.08	-78.8	181.23LOHM	-J 38.48 OHM
220.000 KC	-64.63	-105.6	69.44LOHM	-J 28.63 OHM
240.000 KC	-48.22	-109.3	36.75LOHM	-J 23.33 OHM
260.000 KC	-44.03	-115.6	22.57LOHM	-J 19.90 OHM
280.000 KC	-42.31	-121.0	15.08LOHM	-J 17.46 OHM
300.000 KC	-41.59	-125.5	10.60LOHM	-J 15.62 OHM
320.000 KC	-41.37	-129.3	7.72LOHM	-J 14.17 OHM
340.000 KC	-41.44	-132.6	5.76LOHM	-J 12.99 OHM

FREQUENCY CPS	IND. NETWORK GAIN GAIN	PHASE	INPUT IMPEDANCE REAL	JMAGINARY
360.000 KC	-41.68	-135.5	4.39LOHM	-J 12.01 OHM
380.000 KC	-42.03	-138.0	3.41LOHM	-J 11.19 OHM
400.000 KC	-42.44	-140.3	2.58LOHM	-J 10.47 OHM
420.000 KC	-42.90	-142.3	2.14LOHM	-J 9.85 OHM
440.000 KC	-43.38	-144.1	1.73LOHM	-J 9.31 OHM
460.000 KC	-43.88	-145.7	1.41LOHM	-J 8.83 OHM
480.000 KC	-44.38	-147.2	1.16LOHM	-J 8.39 OHM
500.000 KC	-44.89	-148.6	965.15UOHM	-J 8.00 OHM

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